MAM2024

MARCH 18-21 • MILAN (ITALY)

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FOREWORD

On behalf of the Organising and Scientific Committees, we take great pleasure in welcoming you to Milan (Italy) for this new edition of the Materials for Advanced Metallization International Conference (MAM2024).

MAM2024 will be the 31st in a series of conferences devoted to research on materials and processes for the back and front end of the line, including interconnect and silicide materials.

Starting as a workshop on refractory metals and silicides in the 1980s and moving towards materials for advanced metallization in 1995, the objective of the conference is to provide a forum for open discussions across fundamental and applied sciences and industrial applications.
It is dedicated to international material scientists, process and integration engineers, and students.

Keynote presentations and invited talks will be given by scientific and technical leaders in each of the key areas to present the current state-of-the-art and to stimulate technical discussions.

During MAM2024, a workshop will spotlight Wide Band Gap Materials and Devices, which are revolutionizing industries such as power electronics, renewable energy and electric vehicles. The workshop will present the current state-of-the-art of the technology development and the latest trends in the industry for these applications.

We are indebted to the following Companies for their financial support: Polyteknik, SCREEN Semiconductor Solutions, JX Metals, Applied Materials and Lam Research Corporation.
We also would like to thank all the speakers, exhibitors and participants that joined us in person this year.

Hope to see you again in the next edition of MAM.

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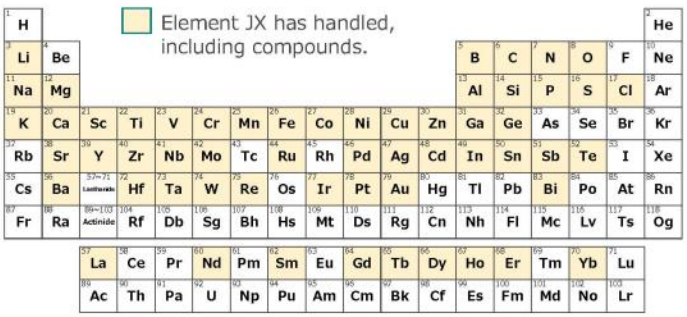

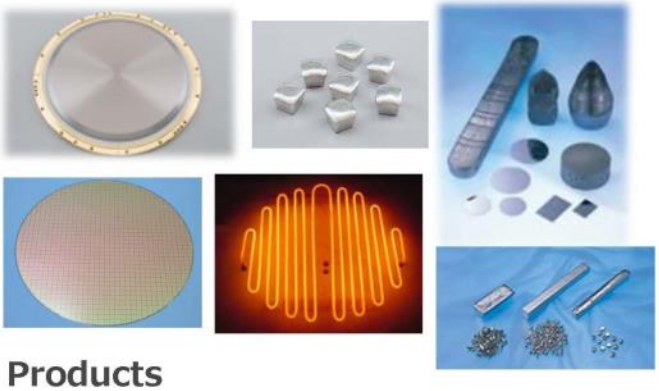

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FREE WIFI	Enterprise Congress Evolution 20
EXHIBITION & POSTERS	Tue. 19 March & Wed. 20 March
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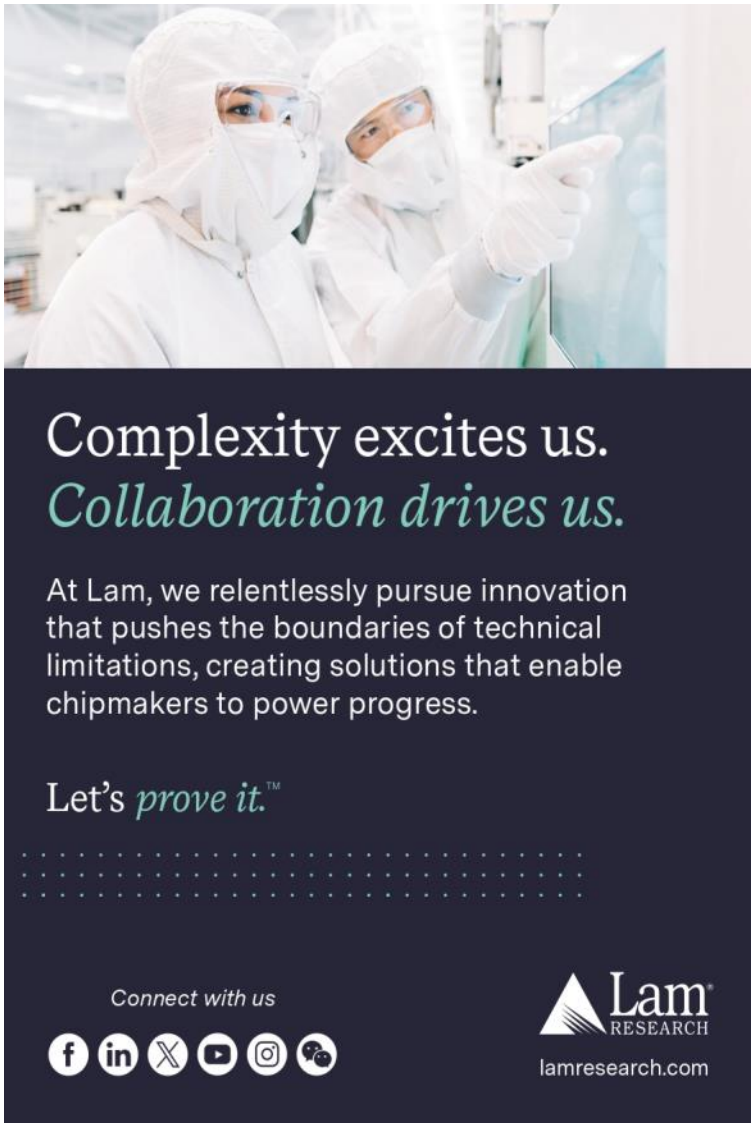

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How STMicroelectronics leverages materials for developing sustainable technologies and Edge AI products

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Discover how STMicroelectronics is leading the way in developing sustainable technologies and edge AI products. Join us for this keynote as we explore the use of advanced materials to address smart mobility, power & energy, and cloud-connected autonomous things. Learn how we're reducing the environmental impact and moving towards carbon neutrality by 2027. We'll also discuss how ST uses responsible materials and processes, such as silicon carbide for automotive and industrial applications, and phase change material for sustainable and secure edge AI products.

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Cyclic etching processes for high selectivity and low plasma induced damage

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The challenges posed by modern patterning processes in micro-nanoelectronics are constantly increasing. In order to meet these challenges, researchers and engineers introduce new materials, evaluate original ways of integrating them and propose alternative processes. Among these, plasma etching remains essential for structuring all the wafers used to manufacture components at a nanometric scale. Used in continuous mode from its introduction in the 1970s until the end of the 2000s, pulsed or cyclic plasma etching processes are now being developed and used industrially at the most critical stages. These processes have been introduced to limit damages, to increase selectivity or to enhance the control of critical dimensions.

In this paper, we review recent developments in cyclic dry etching processes at CEA-Leti. It first briefly reminds the basic principles of plasma etching in microelectronics and then presents various strategies that have been implemented to selectively etch materials without damaging sub-layers or other materials present. These strategies involve alternating steps of adding reactants to the surface, modifying the surface or material to be etched, and removing the modified layers. The alternations can take the form of cycles or supercycles. These approaches will be illustrated by experimental results covering a wide range of applications, including the transfer of patterns formed by direct self assembly lithography [1], gate etching of III-V InGaAs transistor [2], the formation of spacers for advanced FDSOI technologies by cyclic etch [3-6] or topologic selective deposition [7,8], and the etching of contacts on quantum bit architectures on Si. Across all of these applications, the additional benefits provided by cyclic processes will be demonstrated in relation to performance indicators such as damage and/or selectivity. Furthermore, the increasing complexity of developing these approaches highlights the need for a fundamental understanding of each stage of the process. The results achieved in this area will be also discussed in term of plasma-surface interaction to better explain the etching and selectivity mechanisms.

Finally, a concluding section will present the opportunities offered by cyclic plasma etching processes to address the challenges associated with the ongoing development of FDSOI 10nm technology at CEA-Leti.

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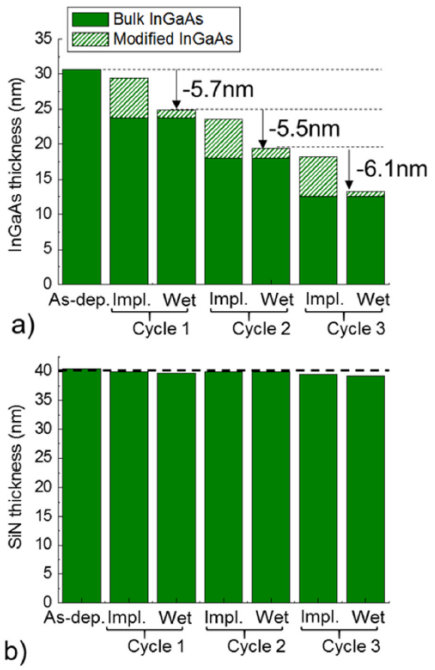

Figure 1 : Evolution of the InGaAs (a) and SiN (b) film thickness after each step composing an etch cycle, from [2]

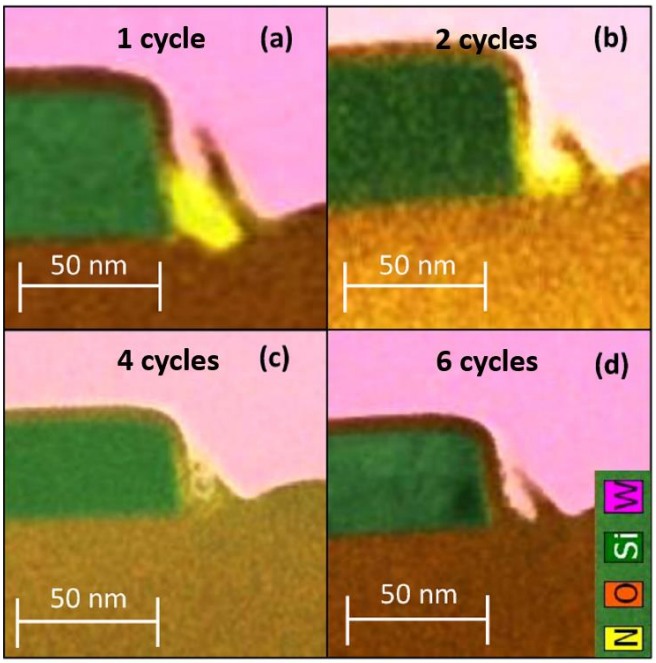

Figure 2 : TEM/EDX images showing the removal of the parasitic spacer on the side of the SOI active area after 1,2, 4 and 6 etch cycles, adapted from [6]

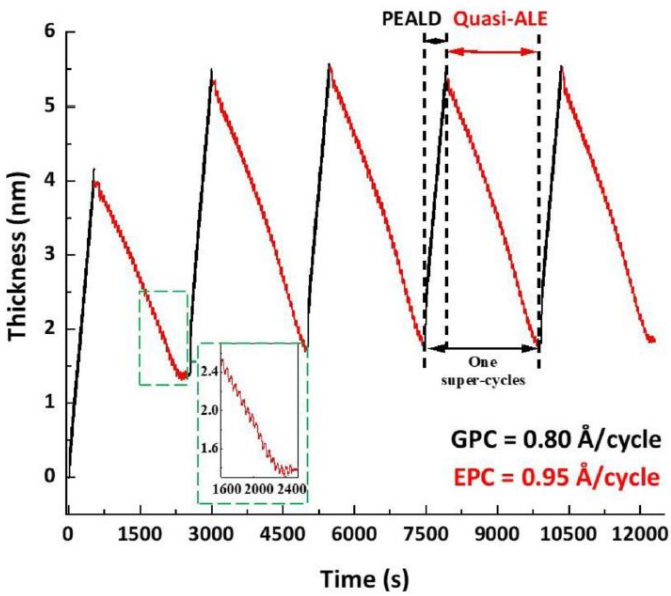

Figure 3 : In situ measurements of five Ta_2O_5 PEALD and quasi-ALE super-cycles on a planar Si substrate, from [7]

Electroplating of Aluminum using Ionic Liquids for Bonding, Via and RDL applications

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Aluminum is often used in semiconductor fabrication due to material and processing properties as well as the CMOS compatibility. Al layers are used as electrical traces, contact pads or passivation material. However, the usage of Al layers thicker than 4 µm is limited. Even though, high-rate sputtering is available and can be used for relatively thick Al layers in range of 10 to 20 µm, the patterning of full area deposited thick Al layers is challenging and causes problems in line-space ratios. For other typical metals, like copper, gold or nickel, electroplating is used to achieve thick and patterned layers by depositing through a resist mask, also called pattern plating. For those metals, water-based electrolytes are used. The electroplating of Al can not take place in water-based electrolytes due to its negative standard potential of E_0=-1.67 V. The water would decompose before a reduction of an Al species occur. Therefore, ionic liquids (ILs) are used for the electrodeposition of metals with highly negative standard potential. ILs are organic salts which can be liquid at room temperature. They offer a wide electrochemical window, low vapor pressure and low flammability. Thus, electroplating with ILs as solvent has gained significant attention in the last 35 years [1,2]. The deposition of Al is reported from different ILs for various application, like corrosion resistance [3,4], thermal and electrical conductivity [5,6] or batteries [7–9]. By introducing the electroplating of thick Al layers on wafer level, new application possibilities open up in the back-end fabrication especially system packaging [10].

The electroplating was developed on 150-mm wafer level from the IL 1-ethyl-3-methylimidazolium chloride (EMImCl) and aluminumtrichloride ($AlCl_3$) in a ratio of 1:1.5. The electroplating process was carried out in a plating unit, which was placed within a nitrogen filled glove box. The inert gas atmosphere protects the IL for moisture and their decomposition. The seed layer changed during the process development from gold to highly doped silicon to Al. The deposition of Al onto Al seed layer is important to achieve a monometallic contact system, thus, reducing process steps and avoiding intermetallic compounds. However, the native oxide of the Al seed layer needs to be removed prior deposition. As the used IL is moisture sensitive, a wet chemical treatment was not possible. Therefore, an anodic reverse pulse was applied to break the oxide and achieve well-adherent Al deposits.

The Al layers were patterned by using pattern plating with different lithography masks for different applications. Firstly, bonding frame deposition for wafer level thermocompression bonding were developed (Fig. 1) [11]. Secondly, pillars for ultrasonic flip chip bonding and thus a parallelization option for wire bonded dies were investigated (Fig. 2) [12–14]. Additionally, the bonding processes were investigated for both applications. The third dimension using vertical interconnects is still under development, but in printed circuit boards and their specific seed layer conditions a lot knowledge is gained to transfer the process to wafer level and semiconductor applications.

Currently, all depositions on wafer level are carried out without any additives resulting in rough surfaces. The future work will focus on additives for an enhanced deposition process and the development of Al alloy deposition to achieve more compatibility to sputter-deposited Al-Cu or Al-Si alloys.

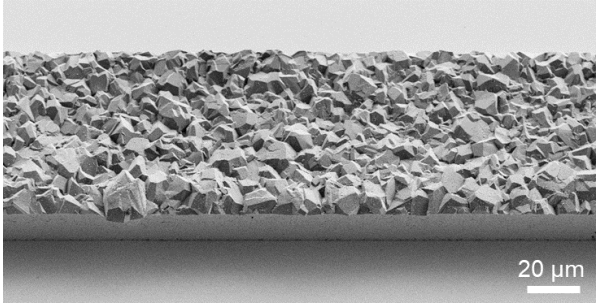

Figure 1: SEM picture of an electroplated Al bonding frame with 60 µm width

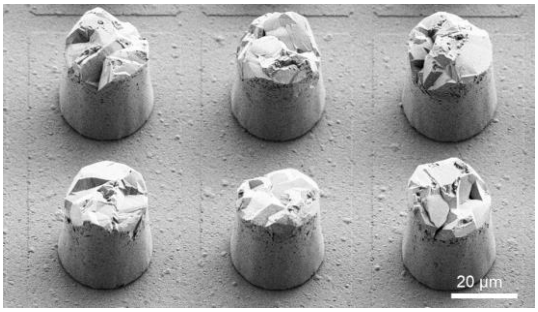

Figure 2: SEM picture of 30 µm diameter Al pillars wiith 50 µm pitch

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Alternative Metallization: Benefits and Concerns

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What are the challenges for Cu metallization?

Cu has been the primary conductor in the logic back-end-of-line (BEOL) stack for over two decades now. For Cu, dual-damascene (DD) is the mainstream integration scheme, where a metal cladding (at the trench bottom and sidewalls) and a dielectric cap (at the top) are needed as Cu diffusion barrier and adhesion layers to ensure, among others, good dielectric and metal reliability, respectively. Scaling the thickness of these layers without compromising reliability is very challenging [1] [2] [3]. Unfortunately, metal barriers are much more resistive than Cu and dielectric caps have higher dielectric constant than the inter-metal dielectric (IMD). Consequently, line resistance, via resistance and interconnect capacitance increase with scaling [4]. The increased impact of electron scattering at interfaces and grain boundaries in narrow features (size effects) further exacerbate resistance trends. Currently, line and via resistance are widely considered to be a performance bottleneck for next-generation integrated circuits [5]. With respect to reliability, electromigration (EM) and time-dependent dielectric breakdown (TDDB) are major concerns for future technology nodes. For Cu, EM J_{Max} drops with scaling, due to smaller critical void size, larger contribution from grain boundaries (grains are smaller), and Cu wires are not expected to withstand the higher current densities required by future designs [6]. Finally, due to the leveling-off of the power supply voltage and increased impact of variability at smaller line-to-line spacing, the electric field that IMD's need to withstand at operating conditions increases with scaling and TDDB reliability margin is expected to reduce dramatically for Low-k DD [7] [8]. Although Cu will still dominate in the intermediate and upper metal levels (fat wires) for many years to come, for the lower metal levels (narrow wires) innovation in materials and processes is key for keeping pace with Moore's law and, at the same time, meeting the performance and reliability requirements which are expected with every new technology generation.

The search for the 'holy grail' metal

Alternative metals to Cu are currently being investigated for the 2nm logic technology node and beyond (metal pitch of 20nm or tighter) to mitigate the degradation of interconnect RC and reliability with dimensional scaling. Metal screening is typically based on figures of merit such as: low product of the bulk resistivity and the electron mean free path for obtaining a lower resistivity at small dimensions (lower R); high cohesive energy for enhancing EM resilience (higher J_{Max}), preventing metal drift into IMD (better TDDB) and enabling barrierless metallization (lower R) [9]; high resistance to oxidation to also get rid of dielectric caps (lower C); low intrinsic stress and good interfacial adhesion for mechanical integrity. Currently, Ru, Mo, Co and W are among the most popular candidates, as they are less disruptive options for the semiconductor industry. Their resistivity is higher than Cu at large dimensions, but size effects are less pronounced and, if barrierless, they can provide lower R than Cu at small dimensions [4]. Furthermore, barrierless via options can significantly reduce vertical resistance (lower IR-drop). Reliability prospects are also better than Cu, because of the higher cohesive energy. Process wise, different options are being considered: hybrid DD, where electroless bottom-up deposition is employed to (selectively) prefill vias with a barrierless alternative metal, followed by conventional Cu metallization; alternative DD, where Cu is fully replaced by an alternative metal in both lines and vias; Semi-Damascene (Semi-D), where direct metal etch is used to pattern a blanket film of (patternable) alternative metal, overfilling vias (to the underlying level) previously etched into an interlevel dielectric. In order to make sensible choices for future technology nodes, benefits and concerns of alternative metallization must be carefully weighed up.

Benefits and concerns of alternative metallization

Hybrid DD can provide better performance and reliability and thus extend the use of Cu metallization, which is strongly pursued by the conservative semiconductor industry. Via-prefill can indeed not only lower via resistance (due to missing bottom barrier and larger metal volume) but also facilitate Cu filling in narrow trenches (vias are already filled), which can in turn be exploited for fabricating taller lines and reducing line resistance as well. As for reliability, EM J_{Max} can be boosted, because (early) via failure modes can be avoided. On the other hand, for barrierless via-prefill metal drift into IMD is a concern for TDDB [10], [11]. Besides, in hybrid DD different metals are in contact, which raises

concerns for thermo-mechanical integrity (e.g. adhesion/delamination), stress migration and metal intermixing [12]. With respect to extendibility, Cu lines are not expected to meet EM reliability requirements at 10nm width and below [6]. Alternative DD can indeed extend reliability [13] [14] [15] [16] [17], but from a performance perspective a one-off improvement is more likely to be expected, as wire resistance would inevitably start increasing again with further dimensional scaling. This calls for more disruptive approaches. In fact, resistance trends could be potentially mitigated by targeting taller lines to compensate for a smaller line width. For DD, that is very challenging, due to trench filling limitations (voids) or dielectric pattern collapse risks (bending, zipping) [18] [19]. In contrast, for Semi-D, that is a viable option, as line aspect-ratio (AR) is controlled by the thickness of the deposited metal film and metal patterns are way stiffer. Besides, larger grains are formed, which further lower resistivity and resistance [20]. Finally, Semi-D is also a very friendly scheme for air-gaps (AG) formation (by non-conformal dielectric deposition) [21], which can be leveraged to contain capacitance increase with AR. Although RC and EM J_{Max} benefits of Ru/AG Semi-D are largely demonstrated and acknowledged by now [22] [23] [24], many concerns still remain. TDDB is no business as usual with Semi-D, because of the innovative subtractive etch process (risks of bridging/shorts) and the additional (possibly weak) interfaces that originate from self-aligned via schemes for variability mitigation [25] [26]. Another concern is joule heating: on the one hand, alternative metals can tolerate high current densities at small dimensions; on the other hand, high currents in narrow (high resistive) lines can induce high temperature [27] and high thermal gradients, which can respectively worsen EM or cause thermomigration (TM) failures in the upper (or connected) Cu metal layers [28] [29]. Self-heating is further exacerbated by the presence of air-gaps, which hinder thermal dissipation [30]. Thermo-mechanical integrity and chip-package interaction (CPI) are further concerns to be tackled [31]. Finally, sustainability aspects must be also considered, accounting not only for raw material cost but also for environmental impact (carbon emission/global warming) [32].

In this talk, we will provide an overview of in-house experimental and modeling work on alternative metallization options, covering among others performance, reliability, mechanical and thermal aspects, and discuss perspectives for future technology generations.

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Advanced Characterisation and Modelling for Degradation Processes in Copper BEoL Stacks of next-generation Power Devices

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In the field of current as well as next-generation power electronics device metallization, understanding and mitigating degradation processes like void formation and cracking in copper (Cu) Back-End-of-Line (BEoL) stacks due to thermomechanical loading cycles is one of the most crucial challenges. This talk focusses on the advanced characterization and modelling strategies aimed at unravelling the multi-physical and multi-scale mechanisms underlying Cu degradation. This leads the path towards enhanced metallization process optimization and advanced lifetime prediction for next-generation power devices.

The presentation will provide an introduction to the criticality of power metallization, highlighting its significance in contemporary technological landscapes. It sets starting point for an in-depth exploration into the methodologies and findings stemming from lab- and synchrotron-based X-ray techniques like nano-X-ray tomography (nanoXCT) with high photon energies as well as Dark-Field X-ray Microscopy (DFXM). These methodologies, combined with in-situ testing strategies, provide unprecedented insights into the structural evolution and degradation phenomena within Cu BEoL stacks, unveiling new facets of the degradation processes and kinetics.

Furthermore, the utilization of advanced electron-probe techniques based on Scanning Transmission Electron Microscopy (STEM) will be discussed in their usage for in unravelling high-resolution details of Cu degradation, like dislocation movement and stacking, offering complementary perspectives to the X-ray methodologies. Through the shown examination and analysis, the electron-based techniques vastly enrich the understanding of the nano- and micro-scale physics of thermal cycle induced Cu degradation and fatigue.

A central aspect of this discourse revolves around the integration of multi-physics and multi-scale simulation frameworks tailored to model Cu degradation. By incorporating mechanical, thermal, and chemical aspects, these simulations offer a holistic view of the degradation processes, enabling comprehensive analysis of the degradation processes and predictive capabilities. The convergence of experimental insights with validated modelling approaches promises to yield towards a robust toolkit for a deep understanding and mitigating of Cu degradation phenomena with unparalleled depth.
In summary, the presented work encapsulates a transformative journey towards comprehensively addressing Cu degradation in power device metallization structures. Through the development of specifically adapted methodologies and workflows rooted in X-ray and electron-based techniques, coupled with the establishment of multi-physics simulation frameworks, a profound understanding of Cu degradation is envisaged. The aimed goals of this studies are not only to optimize metallization processes but also improve advanced lifetime prediction for power devices, fostering a new generation reliable and efficient power electronic devices.

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Si and Mg ion implantation for doping of GaN grown on silicon

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Because of its large bandgap and high breakdown voltage, Gallium nitride (GaN) is a good candidate for high power device applications, as well as Radio Frequency (RF). Moreover, the ability of growing GaN layers on large (200 mm) Si wafers is a key point for its integration in microelectronic lines with reduced costs. Most of the expected applications require n-type and p-type doping of GaN layers. Although, in-situ doping is commonly used during epitaxy growth, ion implantation offers an interesting alternative to enable localized doping for advanced devices. However, the difference in lattice parameters and Coefficient of Thermal Extension (CTE) in the GaN on Si makes the material even more sensitive to the high thermal budgets required to activate dopants after ion implantation.

In the present work, we investigated p-type and n-type GaN doping by ion implantation. GaN layers were grown by MetalOrganic Chemical Vapor Deposition (MOCVD) on 200 mm silicon (111) wafers. To prevent GaN layer surface damaging during high temperature activation anneal, they were capped with an $Al_xGa_{1-x}N$ (or AlN) / SiN_x stack [1].

Silicon is one of the most favorable species for n type doping of GaN. First of all, we showed that the activation efficiency increases with the Si implanted dose (up to $3x10^{15}$ at.cm^{-2}) and that Si does not diffuse significantly at high temperature (1100°C) in GaN. Then, we implanted through a typical heterostructure (AlGaN/GaN) used for High-Electron-Mobility Transistor (HEMT). As shown on Fig.1, we revealed that at high dose ($1x10^{15}$ at.cm^{-2}), the sheet resistance can be reduced in relation to the 2DEG using traditional soak (up to 1100°C) and/or Rapid Thermal Annealing (RTA) (up to 1300°C) which makes the process relevant to improve contact resistance in these devices.

Electrical activation of implanted Mg is still a very challenging subject and, as far as we know, has not yet been demonstrated for GaN grown on Si. The difficulties originate from compensation effects linked to ion implantation induced defects. To understand this phenomenon, we studied the “healing” kinetics of these defects using various physicochemical techniques. Among them, Photoluminescence (PL) measurements were performed to study optical activation of Mg, i.e emission attributed to substitutional Mg in Ga site of the GaN lattice ($Mg_{(Ga)}$). It was revealed that maximizing thermal budgets combining soak anneal (up to 1100°C) and RTA (up to 1400°C) have a beneficial effect on optical activation (Fig.2). PL measurements also showed that Mg implantation leads to the formation of nitrogen vacancies ($V_{(N)}$), which may have a donor behavior. We showed that Mg/N co-implantation reduces $V_{(N)}$ vacancies related emission (Fig.2). Optimization and / or combination of these approaches are then a promising way to obtain electrical activation of Mg implanted in GaN grown on Si.

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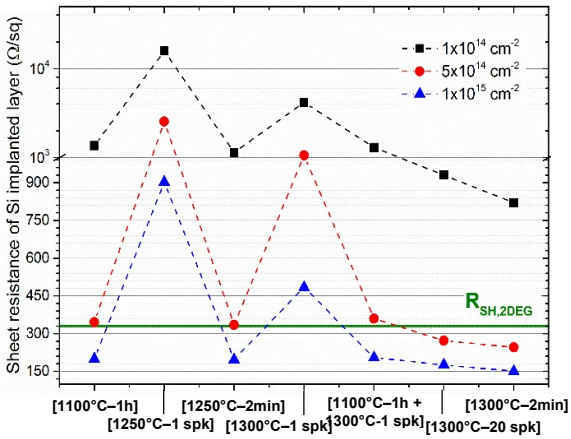

Fig. 1: Sheet resistance as a function of annealing (traditional and/or RTA) for three doses

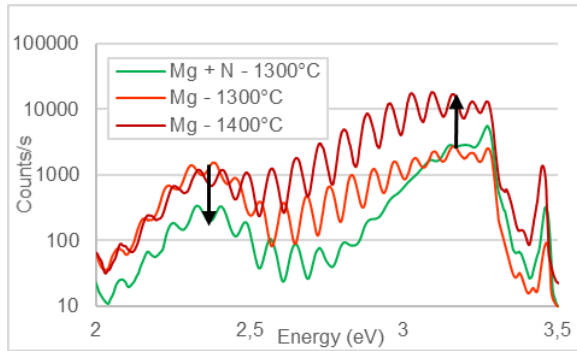

Fig. 2: PL spectra of implanted Mg and Mg+N GaN and annealed with soak + RTA

Simulating conditions for the atomic level processing of metals

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The ambition of atomic level (or atomic layer) processing (ALP) is to be able to control the deposition onto or etching away of atomic thicknesses of a target material selectively at a chosen substrate, and not at other substrates, through the choice of reagent and reactor conditions. In this talk we present a conceptual scheme for the ALP of metals [1] and a simulation approach to find which conditions to use for each type of deposition or etching.

In the general case, four types of process are conceivably in competition when a metal surface is treated with any reagent or reagent-combination: continuous deposition (CVD) or etching, or self-limiting pulsed deposition (ALD) or etching (ALE). We show that first principles thermodynamics based on density functional theory (DFT) of bulk and surfaces is a computationally-efficient approach for distinguishing between the four processes. Crossover temperatures and pressures can be estimated, with the accuracy depending on how entropy, coverage and diffusion are treated.

We use the example of ruthenium metal to illustrate the simulation strategy. Ru continues to be investigated as a possible seed layer for interconnect electroplating in the fabrication of electronic devices. Ru can also be used as a capacitor electrode and as a heterogeneous catalyst. Ru was one of the first noble metal ALD processes to be discovered [2] and, coincidentally, Ru oxidation was the subject of a pioneering exposition of DFT thermodynamics [3].

Ru metal or RuO_2 can be either deposited or etched depending on exposure to oxidants (O_2, O_3, O_2-plasma) or reductants (H_2 and a variety of Ru precursors) [4]. Quasi-catalytic cycling between metal and oxide is key to the deposition mechanism [5]. RuO_4 gas can play the role of deposition precursor or etch product, with the mechanism of etching recently computed by Shong *et al.* [6]. Low-temperature deposition allows substrate-selectivity, which can be enhanced by punctuating the process with an additional self-limiting etch step [7]. We therefore focus on the conditions for self-limiting versus continuous ALP of Ru metal, hydride, hydroxide and oxide with respect to H_2 and RuO_4 reagents.

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Memory Technology enabling the future computing systems

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More than 2.5 exabytes of data are created every day demonstrating that we entered in the Data Economy Era, unlocked by the development of more and more advanced memory and storage technologies. The exponential growth of the annual volume of data generated in the global Datasphere (Fig. 1) is predicted to be strongly fueled by the more and more pervasive growth of Artificial Intelligence (AI) and 5G, forming a powerful duo of the data economy.
AI fundamentally re-defines the insights we can deliver through data.
5G, at variance, is unleashing data movement, asking for low latency and enhanced mobile bandwidth.

This new scenario demands that also the underlying computing system infrastructure is re-architected from the ground up to optimize for *data centricity*.

The access to these vast pools of data is exacerbating the limitations of the speed and energy that is consumed during the transfer of data between the memory and the CPU. In other words, memory, the enabler of the Data Economy, is now becoming the bottleneck. Thus, new approaches, inspired to the human mind, are essential for creating more efficient computing systems evolving towards a data-centricity and extending to the intelligent edge. Definitively, the integration of Compute and Memory can address the "Memory Bottleneck" by means of the:

1. Insertion of a "tightly" compute coupled layer in the Memory Hierarchy
2. Moving compute primitives onto the memory die
3. Merging the compute and memory with in-memory Neural Network fabrics

Emerging Memories and Memory Abstraction are likely further enablers for a solution of the "Memory Bottleneck".
Fig. 2 reports the prismatic decomposition of the AI semantic, meaning: Neural Network accelerators, Deep Learning, Matrix-Vector-Multiplications, Brain-inspired neural Network using spikes to transmit and store information, In-memory Logic, Associative memory and storage,…

The talk will highlight as the breakthroughs in interconnect technology is pivotal to optimize the link between Host and Memory and, thus, to fulfil the various In-Memory-Computing applications.

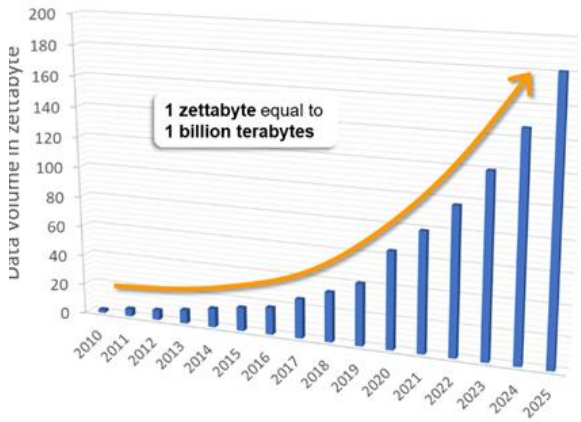

Figure 1: Annual Size of Global Datasphere over time (in ZB) and its projection up to 2025. *Source: IDC Global DataSphere report 2021.*

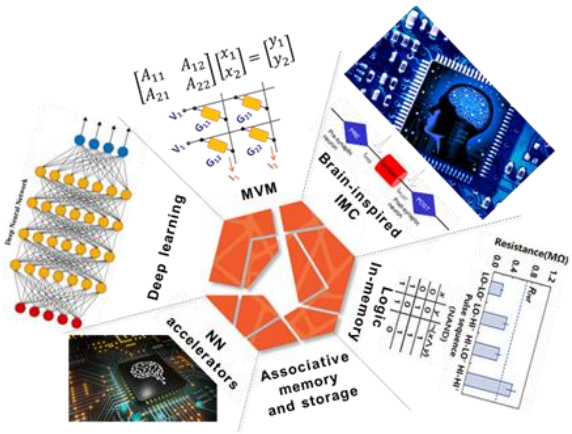

Figure 2: Various In-Memory Computing applications required for a computational memory.

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Strain and lattice tilt mapping of GaN on Si nanowires at early stage of coalescence by synchrotron x-ray nano diffraction

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Gallium nitride (GaN) is a very attractive III-V semiconductor for optoelectronics applications and it is highly relevant for the fabrication of light emitting diodes. Epitaxial growth of GaN is nevertheless expensive due to the substrate cost and size limitations. Thus, growing GaN on low-cost foreign substrates is more common, however, the GaN layer will present many dislocations reducing the emission efficiency. We aim to improve the quality of the epitaxial GaN layer by developing an original method based on growing GaN pyramids on top of GaN/AlN/Si(111)/SiO_2/Si(001) etched nano-pillars [1]. At high growth temperatures, viscoelastic properties of SiO_2 will allow deformation, which should let the pillars undergo a rotation and allow the GaN on top to coalesce into 40x40 µm² platelets with no boundary dislocations. In this work, we combined two x-ray microscopies techniques at the state of the art to gain a deeper comprehension of the GaN coalescence at an early stage.
In a first study we used Dark-Field X-ray Microscopy (DFXM) on beamline ID06 of the European Synchrotron Radiation Facility (ESRF). DFXM is a non-destructive imaging technique that can provide three-dimensional (3D) maps of microstructures in crystalline matter. The whole GaN structure is illuminated with focused monochromatic X-rays and the diffracted beam then passes through a compound refractive lens (CRL) placed after the sample to produce a 10x magnified real (x, y) image on the 2D detector. Combined with a phi (Φ) or omega (ω) rotation of the sample, these scans provide information on the crystallographic mis-orientations in the sample, specifically the tilt and twist of the crystallites. Thanks to DFXM, we show that extremely well oriented lines of GaN (standard deviation of 0.04°) with low dislocation densities [2] as well as highly oriented material for zones up to 10 x 10 µm^2 in area are achieved with this growth approach. Complementary macroscopic high intensity X-ray diffraction shows that the coalescence of GaN pyramids causes dis-orientation of the silicon layers in the nano-pillars, implying that the growth occurs as intended. Then, to go deeper into the mechanical behaviour of the GaN layers and of the Si pillars, we completed this study by using scanning diffraction x-ray microscopy (SDXM) on beamline ID01 at the ESRF. By performing x-ray diffraction measurements using a two-dimensional detector and a nano x-ray beam (~40 nm), we obtained (Q_x,Q_z) reciprocal space maps around the asymmetrical GaN (105) Bragg reflection at every (x,y) position of the sample and thus obtained the GaN lattice tilt, strain and peak broadening at each position We used SDXM on a reference sample with uncoalesced GaN nanopillars, and on a second sample at the early stage of coalescence (not fully coalesced). The results show that the disoriented GaN pillars have transformed from a large distribution of orientation into bigger well-defined domains of GaN very well-oriented within themselves. In addition, a broadening of the peak along Q_z and a higher strain value were detected at the borders of the same grains identified in the tilt map.
These results will be discussed in terms of mechanisms at work during the early stage of coalescence and optimization of the growth process (pillars pattern, size…). Although it was not possible to achieve highly oriented GaN layers in every case, we show that this growth technique is extremely promising for micro-displays or micro-LEDs, which require small islands of high quality GaN material.

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Fundamental issues of wetting and interfacial reactivity in electronic packaging

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3D integration is a modern way for electronic packaging where devices are stacked on top of each other or packaged. The electrical, optical and thermal connections are made between the stacks and package using interconnects. Soldering is the most common way of interconnecting electronic components and it is applied at all levels of integration in electronic packaging industry [1, 2].

Multiple reflows for solder/substrate contacts are widely used in 3D electronic packaging. During a reflow, several processes occur such as melting of the solder, wetting of the substrate by the liquid solder, interfacial reaction at the solder/substrate interface and solidification of unreacted solder. Each of these processes can play a crucial role on the subsequent evolution of the joint, and their control becomes more and more complex with the continuing trend towards increasing miniaturization.

Nowadays, copper is the most common conductor metal used in contact with solders owing to its good solderability characteristics. Commonly, in order to reduce the growth kinetics of intermetallic (IMC) layers at the liquid solder/Cu interface, a Ni barrier is introduced between Cu and the solder. Moreover, in order to protect Ni (or other metal) surface from oxidation, a thin Au layer is deposited on the metal surface. Sn-based solder alloys are the most popular lead-free solders used in the microelectronic packaging industry. However, for specific applications, other solder alloys are often used such as In based alloys or eutectic Au-Sn, Au-Si and Al-Ge alloys, etc.

A good wetting, contact angle well below 90°, is a necessary condition to obtain a good interfacial adhesion and therefore a good joint after the soldering process. The most common solder/metal substrate systems are reactive systems, i.e. with formation of fragile IMCs. Thus, the IMC layer formed at solder/substrate interface may adversely affect the mechanical properties of the joint. Moreover, this layer can play a major role on the undercooling degree of the liquid solder during the cooling process and thus on the final microstructure of the joint and its mechanical properties. Therefore, the morphology and thickness of the reaction layer should be controlled by monitoring the solder alloy composition and impurities, oven atmosphere, temperature and reaction time.

This presentation focus on the fundamental aspects of wetting and interfacial reactivity as well as on their interrelation during soldering process involving different solder alloys such as eutectic Au-Sn [3-5], Sn based alloys [6-16], eutectic Al-Ge [17], pure In [18] and different metal substrates such as Cu [6-10, 12, 15, 16], Ni [13, 14], Ag [11] and Au [3-5, 17, 18]. The relationship between wettability and reactivity in metal/metal systems is presented and discussed from a general point of view.

Wetting and spreading kinetics of metallic droplets on solid metal surfaces are studied by using the transferred drop technique in a metallic furnace under high vacuum ($P \sim 10^{-7}$ mbar) and a rapid camera (1500 frames/s). Figure 1 gives an example of variation of the contact angle and the drop base radius during spreading of liquid In on Au substrate at 300°C. In order to determine the different stages of the spreading kinetics (non reactive and reactive spreading regimes), specific experiments on the bulk IMC compounds are also performed. As an example, figure 2 compares spreading kinetics of liquid Sn on Cu substrate to that on a premade bulk Cu_6Sn_5 substrate. Finally, as usual metals are covered with thin native oxide layers which are not wetted by liquid metal alloys, the role of heat treatments at high temperature under vacuum and that of intense reactions occurring at the oxidized solid/liquid alloy interface on the final degree of wetting are presented and discussed.

In the second part of the presentation, we discuss some fundamental issues of interfacial reactions between different solder alloys and metal substrates in the light of specific experimental results. First, the role of the reaction product microstructure on the growth mechanisms and growth kinetics of IMC layers is clearly established by carrying out specific experiments. As an example, figure 3 compares the differences between the interfacial reactivity of Cu with the metastable Sn-0.7wt%Cu liquid alloy and Sn-0.7wt%Cu solid alloy at a rigorously identical temperature. Second, the evolution of the morphology and the average thickness of the reaction layer with time and experimental temperature is

presented and discussed for different solid/liquid diffusion couples - an example is given in figure 4 for Ni/liquid Sn system. Finally, the differences in the morphology and growth kinetics of the reaction layer at liquid solder alloy (A)/metal substrate (S) interface, due to the initial conditions of contact between them (immersion of solid S in liquid A or deposition of a layer of A on the surface of S), are highlighted on the basis of experimental results and microstructural analysis.

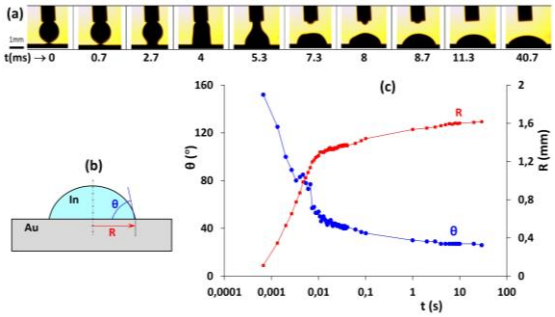

Figure 1 (a) Some images of In droplet during its spreading on Au at 300°C. (b) Definition of the contact angle θ and the drop base radius R. (c) Variation of θ and R during spreading.

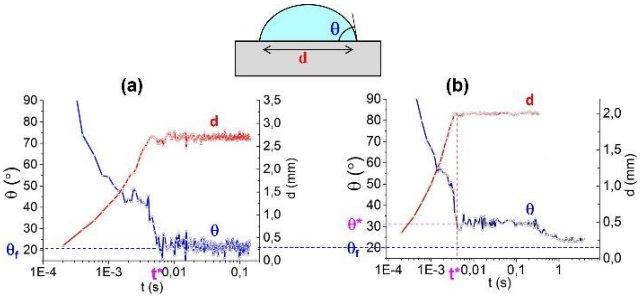

Figure 2 Variation of the contact angle θ and the drop base diameter d of Sn-7.8wt%Cu droplet during its spreading on Cu_6Sn_5 (a) and Cu (b) substrates at 390°C.

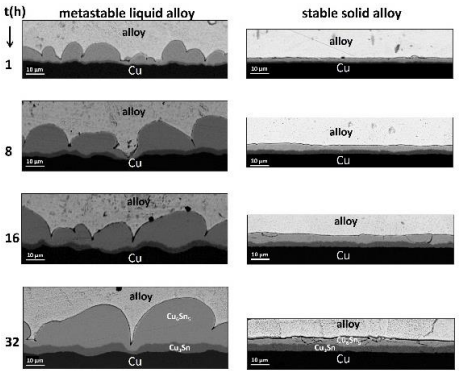

Figure 3 SEM micrographs of the reaction product formed at Cu/metastable liquid Sn-0.7wt%Cu alloy and Cu/solid Sn-0.7wt%Cu alloy interfaces for 1 to 32 h at 222°C.

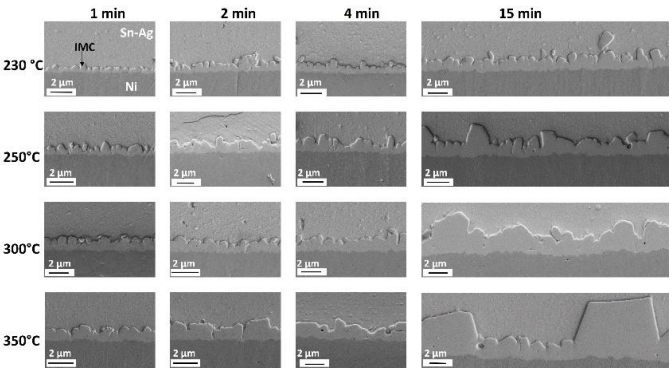

Figure 4 SEM micrographs of the reaction product formed at the Ni/liquid Sn-2wt%Ag interface for the samples aged for 1 to 15 min at 230 to 350°C.

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Overview of Inline Metrology Challenges in IC manufacturing environment

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It is widely acknowledged that inline Metrology is a powerful enabler that speeds up the introduction of new technologies, secures the ramp-up of pilot lines, and improves yield in mature factories. Inline Metrology reduces the cost of manufacturing and development by providing valuable and extensive characterization of processes and products directly at the manufacturing line. Over the years, as technology requirements became more demanding, inline metrology had to constantly evolve and adapt to keep up with shrinking dimensions, atomic-scale layer thickness, and new 3D architectures. The increasing demand for ICs in the automotive market has led to a reinforcement of quality requirements associated with measurement system and product control plan management. Therefore, one of the major challenges in metrology is to maintain the level of performance for the key criteria, namely accuracy, sensitivity, stability, capability, and productivity, over the years.

From a technical perspective, classical inline metrologies, which were mostly based on optical techniques and scanning electron microscopes, have been reaching their limits since the development of More Moore technology nodes below 45nm. To measure thin and ultra-thin films, the industry had to rapidly adopt X-Ray based techniques such as XPS, HRXRD, and XRR, which were traditionally restricted to offline laboratories. To measure Optical CD, the complexity of 3D pattern structures has led to the introduction of Muller matrix and the combination of multiple optical modules for model fitting, while overlay techniques have moved from image-based to diffraction-based techniques. Overall, metrology techniques have continued to evolve towards more complex model-based techniques that support multiple physics and multi-scale parameters. On the other hand, for More than Moore applications, the introduction of a large number of new materials and the adoption of complex 3D stacking architectures have led to the emergence of new requirements, such as mechanical and thermal properties, adhesion strength, and piezoelectric characteristics (Fig.1). In general, industrial metrology solutions can be found by adapting existing laboratory techniques to fulfil industry standards and/or by creating prototypes through common development between IC makers and key suppliers from the sector. This collaborative approach is particularly important for inline metrology because all contributors share the same need for an anticipatory approach to ensure that adequate control methods are ready ahead of process qualification steps.

To push the limits further, other methodological approaches such as feed-forward strategies and Hybrid metrology (combining data from complementary techniques) have also been explored [1]. In the context of industry 4.0 evolution, metrology techniques themselves, and more specifically the way information is extracted from the given signal or image, are also evolving. With the introduction of Neutral Network and Deep Learning algorithms, the raw signal can now be exploited in a different way to extract the maximum level of information from a measurement step [2]. Metrology can now be applied to detect anomalies (for example, Good/Bad categories) rather than just extracting precise physical or chemical quantities [3]. In this context, the borders between metrology and defectivity activity domains are blurring, opening the door for the Metro-Spection concept (Fig.2). As a result, metrology, which still requires a background in SC fabrication, process, measurement technology, and physics, is now expanding its required skills to include data science for quick adoption. Some relevant application use cases related to MetroSpection will be presented and discussed in the oral presentation.

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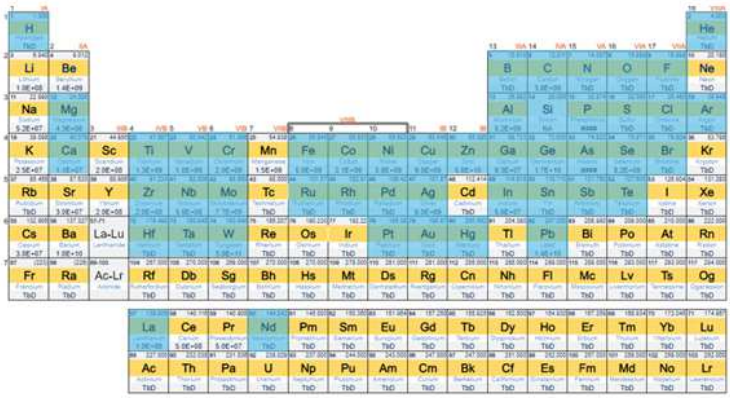

Figure 1: Example of chemical elements introduced in IC manufacturing (highlighted in blue).

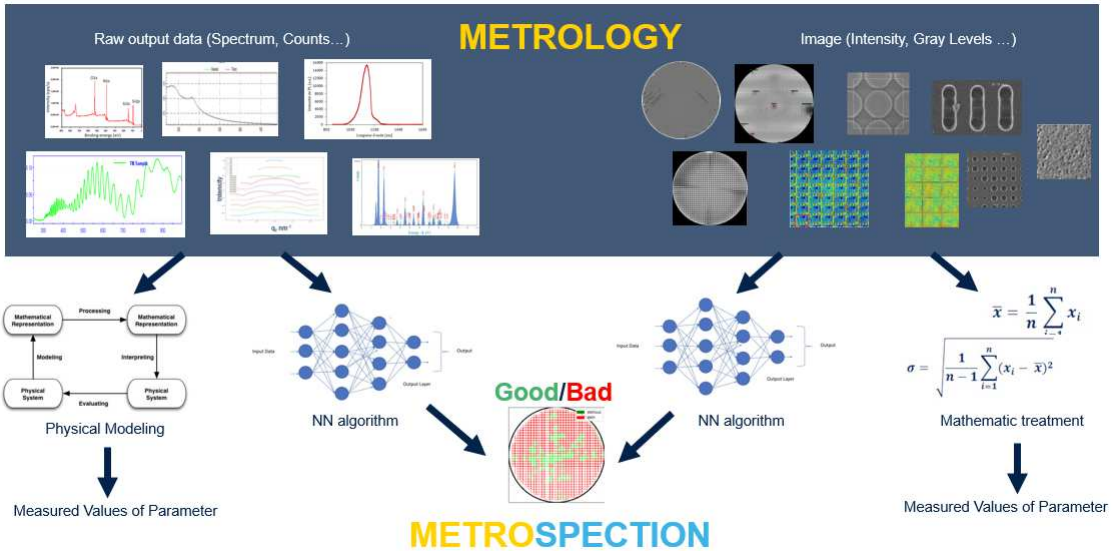

Figure 2: MetroSpection Concept. Metrology raw outputs being used for Good/Bad assessment.

Low energy electron microscopy: from basic principles to surface dynamics of semiconductors

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In this presentation, I first discuss the basic principles of low energy electron microscopy (LEEM). I describe the main imaging modes of material surfaces by LEEM using the reflected and diffracted electrons by the surface. This overview is complemented selecting the most important related techniques to address crystallographic, magnetic and chemical properties using respectively LEED, spin-polarized LEEM and PEEM techniques. In a second part the major advantages of LEEM are addressed: the possibility to study in real-time the spatio-temporal dynamics of surfaces under non-equilibrium conditions through selected examples in the context of semiconductor physics. The thermal de-oxidation [1-3] and the solid state dewetting of silicon [4,5] on silica (Silicon-On-Insulator, see Fig.1) are quantitatively studied, taking advantage of the multiscale imaging potentialities of LEEM. Then I will focus on the growth of metallic eutectic nanodroplets on silicon surfaces, as seeds for nanowire growth [6,8]. At last it will be shown that LEEM allows addressing electro- and thermo-migration processes at surfaces with unprecedented accuracy by measuring the drift velocity of single atomic step edges [9-12].

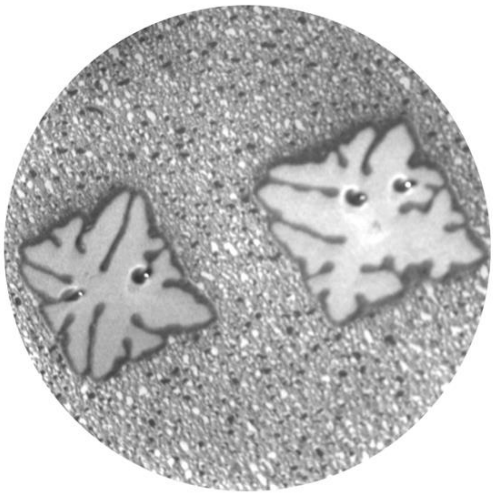

Fig. 1: LEEM image of Silicon-On-Insulator surface during solid state dewetting at 850°C. Field of view: 25 µm.

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Direct Metal Etch and Semi-Damascene Integration of Ruthenium: A Game-changer for interconnects

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Alternative materials and integration processes as a replacement for Cu Dual Damascene have long been under scrutiny within the interconnect research communities. Reducing resistance and capacitance stands as a pivotal challenge in enhancing interconnect performance for forthcoming technology nodes. Ruthenium (Ru) emerges as a resilient contender at the metal level, diverging from Cu, owing to its resistance to oxidation, elevated melting point, low bulk resistivity [1], and the absence of a necessary metal barrier. Additionally, Ru facilitates subtractive metal semi-damascene (Fig.1) with notable integration advantages: (1) direct metal etch enables high aspect ratio (AR) patterning (Fig.2). This alleviates the constraints associated with trench filling, permitting resistance reductions at equivalent metal pitch (MP) [2,3] (Fig.3). (2) This methodology affords precise control over the height of patterned lines by adjusting the thickness of the deposited metal and the etch process, removing the need for a metal CMP [4,5]. (3) Below 22nm MP, a fully self-aligned via (Fig.4) becomes imperative to prevent via-to-line leakage [6,7].
This proposed scheme utilizes a semi-damascene integration sequence: the first metal layer is formed through subtractive metal etching. Subsequently, a highly selective etching process is employed to construct the via on top of a lower metal line by removing its hard mask (HM). The next metal level is then established using subtractive metal etching. A pioneering demonstration of 2-metal level (2ML) devices using subtractive metal etch with Fully Self-Aligned Via (FSAV) was presented by Murdoch et al. [8] (Fig.5). Subsequent enhancements in etch and cleaning procedures laid the groundwork for the subsequent implementation FSAV high yielding [9]. In this presentation, we will delve into the intricate details of utilizing subtractive patterning with Ruthenium to implement the semi-damascene scheme—an innovative approach recommended by imec as a viable alternative to Copper (Cu) damascene in advanced logic nodes.

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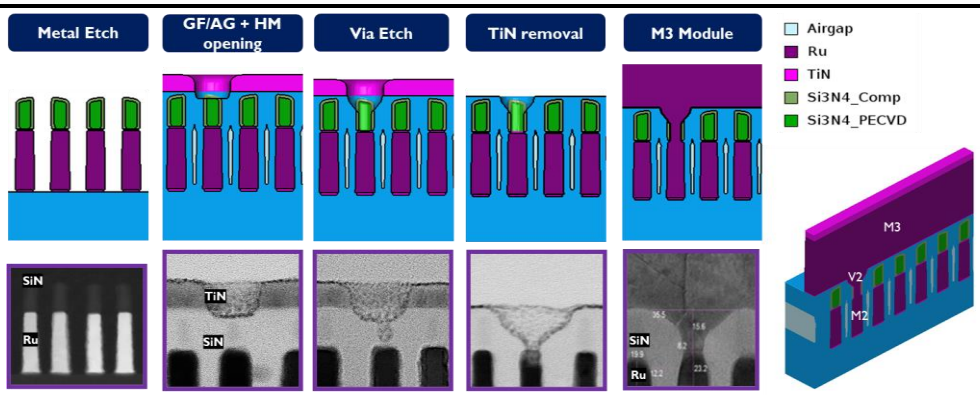

Fig. 1: Integration scheme for semi-damascene 2ML FSAV.[9]

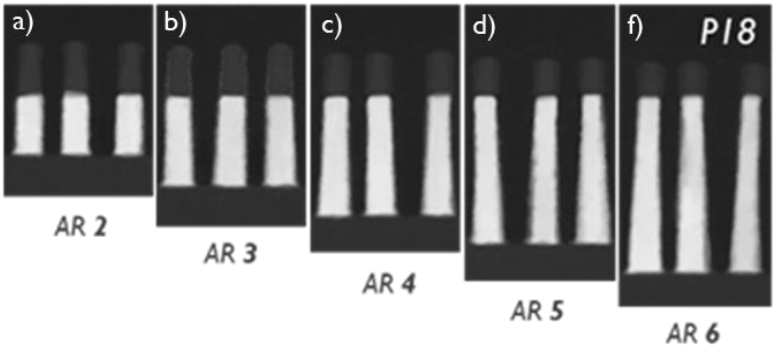

Fig. 2: a) Cross-section TEM of MP18 Ru lines with various AR (a) 2, (b) 3, (c) 4, (d) 5 and (f) 6, demonstrating a nearly vertical profile of the Ru lines and the scalability of current scheme towards higher AR. [2]

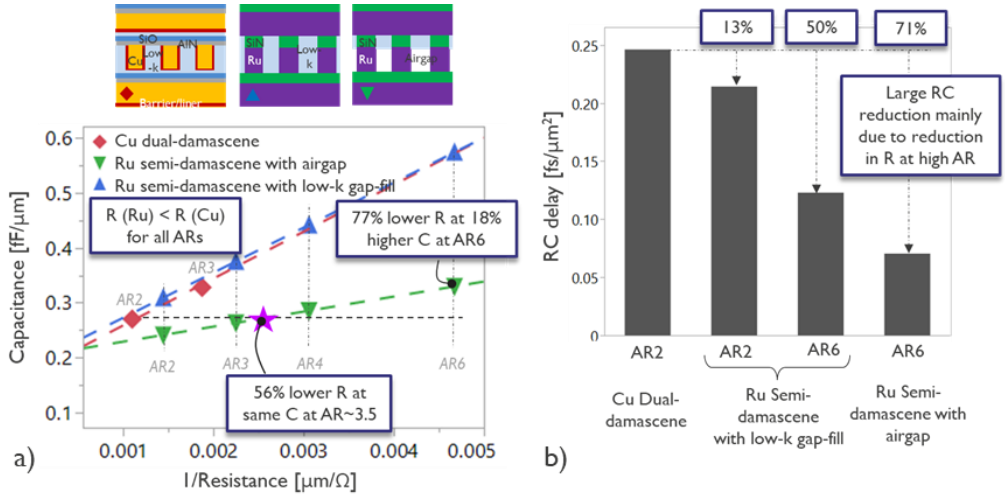

Fig. 3 3-metal-level TCAD evaluation comparing Cu-dual damascene (DD) vs Ru-Semi-damascene (SD). (a) Compared to AR2 Cu-DD, AR2 Ru-SD with airgap offers a significant, 24% lower C, while AR6 Ru-SD with airgap have comparable C. (b) RC delay product shows 13% lower RC with Ru semi-damascene thanks to lower film resistivity and barrierless Ru compared to Cu with 2 nm barrier/liner. Possibility to fabricate high aspect ratio Ru lines with airgaps in semi-damascene can lower the RC further by 71%. TCAD evaluation is carried out using imec resistivity model [9] on 10 nm width and MP18 nm 3-metal configuration as shown in the schematics.[3]

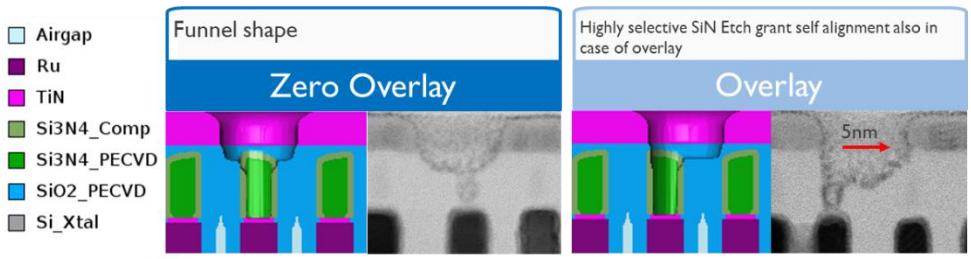

Fig. 4: Fully self-aligned model and cross-section TEM in case of zero x-shift and 5nm x-shift.[9]

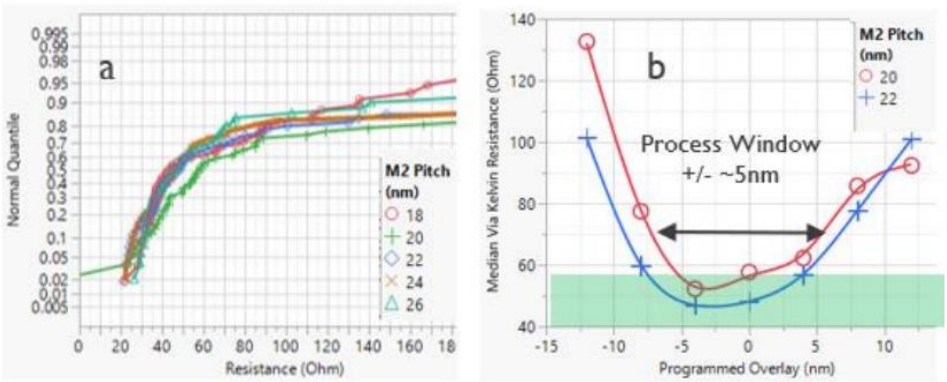

Fig 5 a) Via Resistance from 18-26nm MP and b) median via resistance vs programmed overlay for MP20 and 22nm.[8]

Low damage Etching processes developments for GaN-based devices patterning

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Gallium Nitride becomes more and more present in various microelectronic applications thanks to its different interesting properties. Its crystallographic (wurtzite cell) and thermodynamic parameters are exploited for the new generation of Power (High Electron Mobility Transistor "HEMT" and Diode) and RF devices, to support high voltage, high current, high operating temperature and frequency [1]. On another hand, its direct wide-band gap (3.4eV) permits the GaN to be a good material for photon emission, and therefore is exploited into LED, microLED and displays.

The fabrication of these different GaN-based devices is not trivial, as some processing steps – especially plasma etching – can be critical for the GaN material integrity, affecting the final device functioning. For the patterning step, the most important requirement is the use of **low-degrading plasma processes**. For "pGaN gate" and "Recessed-gate" HEMT, electrical performances are directly linked to GaN damaged, especially at gate bottom [2]. For LEDs, a particular attention on pixel sidewalls is needed to limit damages and maximize the photon emission [3].
Moreover, depending on the application, GaN etching step need to comply morphological requirements. For instance, pGaN etching need to be selective to the underneath AlGaN barrier layer in "pGaN-gate" HEMT devices [4], vertical profiles need to be obtained in "Recessed-gate" transistors and LEDs, and a perfect control of the etching rate is needed for partial etching of few nanometres of thin AlGaN barrier in RF HEMTs.

In this talk, we describe different studies and plasma approaches done at Leti to address those challenges. The understanding of GaN etching and degradation mechanisms was investigated to identify and focus on key-parameters, for each application. To reduce Plasma-Induced damage, GaN Atomic Layer Etching [5] was implemented for low-degrading plasma solution to improve Power devices properties. As described in Fig. 1, the added degradation brought by plasma etching is reduced using ALE Cl_2/Ar process, compared to the ICP RIE reference. The ALE chemistry is an important parameter we studied, as the use of Helium instead of Argon which shows higher degradations [5]. By nature, ALE and cycling processes lead to very slow etching rates. Therefore, other low-degrading technics with better throughputs have been studies, such as bias pulsing or Quasi-ALE.
To also better comply with morphological criteria, the impact of plasma parameters and etching environment on profile were studied. The Fig. 2 reports the study of the GaN etching mechanism in a Cl_2/BCl_3 RIE process with a photoresist mask. The chemical analysis of remaining byproducts on sidewalls (containing Cl, C and Ga traces) and a plasma parameters parametric study allow us to propose a mechanism ruling the sidewall passivation phenomenon, and to tune the process to optimize the etching profile (more vertical). The same investigation has been also done for etching using hard mask (SiO_2, SiN) for comparison.

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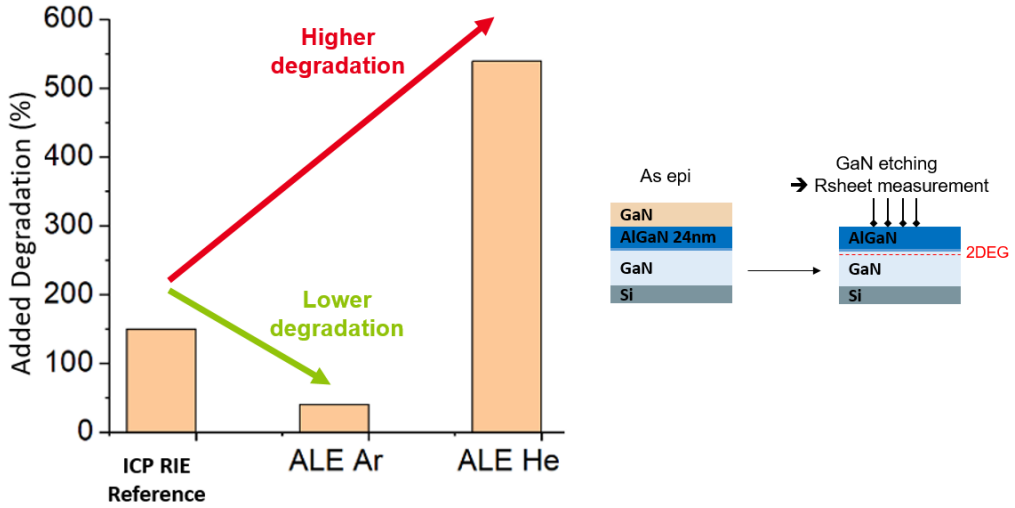

Fig. 1 : Added degradation measured by R_{sheet} after GaN etching by ICP RIE reference process, compared to ALE Cl_2/Ar and ALE Cl_2/He processes

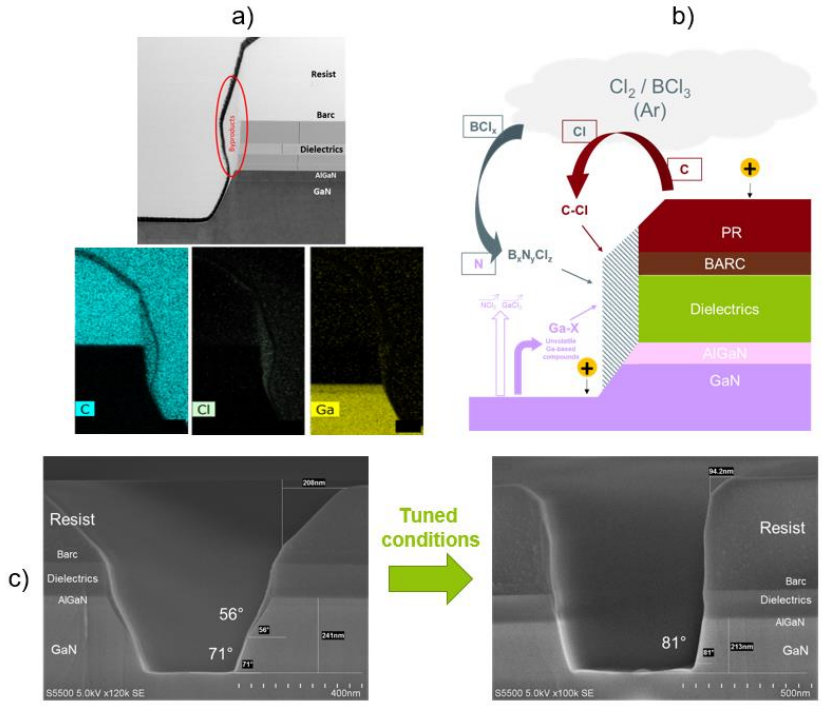

Fig. 2 : Morphological study of GaN trench etching in Cl_2/BCl_3 - based process with a photoresist mask. Chemical analysis of post etching sidewall byproduct (a), proposal of a mechanism for sidewall passivation (b), and finale profile optimization (c)

Resistive switching memories for spiking neural networks

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Resistive switching memory technologies (RRAM), also named as memristive devices, are graining increasing attention for implementing unconventional computing concepts, such as in-memory and brain-inspired computing [1]. RRAMs are very promising because of low power consumption, scalability down to nm scale, CMOS compatibility and capability to support in-memory computing in neural networks, then overcoming the limit of the von-Neumann computing architecture. Moreover, RRAMs can serve as dynamic elements exhibiting useful neuromorphic functionalities such as analogue control and evolution in time of their conductance values as a function of input stimuli. Today, RRAMs are becoming promising compact building blocks in hardware spiking neural networks (SNNs) to reproduce the synaptic or neural functions, and their rich dynamics is used to build circuits and systems able to processes information with temporal structure and compute over multiple time scales, mimicking the brain functionality. In the medium to long perspective, RRAMs can substitute and/or complement CMOS circuits in future neuromorphic chips [1-3], also towards low-power computing systems for edge applications, such as the ones relying on smart analysis of sensory signals in real time.

In this work, we will first introduce the current state of the art and role of RRAMs and memristive systems in neuromorphic computing with focus on materials systems and types of devices under investigation to implement the synaptic and neural functions; and we will discuss device requirements versus SNNs implementation. In the second part, we will show our recent results in the field of RRAM devices, featuring a metal/insulator/metal stack device structure, for neuromorphic applications. We will show how RRAMs, depending on the used material stacks and programming strategies, are used to implement neuromorphic functionalities, such as analogue dynamics response to input stimuli [2-5], and controllable stability of the device resistance states over various time scales. We will also show how memristive devices can function as volatile or non-volatile dynamic memory elements mimicking the short/long term plasticity of biological synapses. As example, we engineered both analogue non-volatile HfO_x-based RRAM as synaptic nodes in SNNs, and Ag/SiO_x- or Ag/Al_2O_3/SiO_x-based devices with tunable retention properties (from µs to tens of seconds), and exhibiting a conductance modulation as a function of trains of input spikes.

To summarize, we will show how diverse types of RRAMs, relying on different material stacks and mechanisms, can be engineered for neuromorphic computing with focus on SNNs hardware implementation. We will discuss on materials stacks, device characteristics and underlying physics, and finally we will further analyse how to exploit device properties in hybrid CMOS/RRAM neural networks through system-level simulations [6-8].

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Controlling Ni silicide formation by ion implantation

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Given its importance as contacting material, the formation of NiSi via the reaction of a Ni thin film with a Si substrate has been thoroughly investigated during the past decade. In order to keep up with the requirements imposed by the aggressively shrinking device dimensions, extensive efforts have been devoted to optimally tune the silicide properties in terms of resistivity, formation temperature, texture, thermal stability, etc. Approaches which have been taken include, amongst many others, alloying of the Ni with Pt or Pd. On the other hand, it has also become clear that the transient, metastable phases which appear during the early stages of the Ni-Si reaction, have a crucial impact on the reaction path, hence on the properties of the final phase of interest, i.e., NiSi.

To disentangle the role of these metastable silicides, we have focused on the use of ion implantation, a standard technique in device processing. The role of implantation is dual: on the one hand, it introduces impurities in the matrix (dopants), while on the other hand, damage (lattice defects) is created as a result of atomic collisions. Understanding the specific impact of impurity atoms and defects on the kinetics and/or thermodynamics of the silicide reaction path will allow one to tailor the metastable phases initially formed, and therefore the NiSi properties.

In order to differentiate between the various irradiation-induced effects, we have implanted either nitrogen (impurity) or argon (creating defects) to a range of fluences. The implantations were performed prior to thermal reaction, with an energy adjusted to either target the Si substrate, the Ni layer, or the interface region [1,2].

In this talk, we will focus on two metastable nickel silicide phases, i.e., the hexagonal Ni-rich phase (θ-phase) and the amorphous $Ni_{0.5}Si_{0.5}$ alloy, and review how these phases can be either stabilized or destabilized by ion implantation. To this end, we will detail on the specific role of the implantation-induced defects and the impurity atoms (i) on the phase formation sequence, (ii) on the reaction kinetics and (iii) on tuning the texture of the NiSi film (which has a major impact on the NiSi stability). We have found that these properties are to a large extent determined by a subtle interplay between the impurity concentration at the reaction front, their solubility in the various silicides, the occurrence of additional nucleation barriers, the grain orientation, a suitable template depending on the Si crystallinity… as well as the annealing conditions [1,2]. As an example, Fig. 1 shows how N implantation can result in the formation of an amorphous Ni-Si silicide, whereas Fig. 2 illustrates the impact of Ar implantation on the silicide formation temperature.

To disentangle the details of the silicidation, we have relied on a number of complementary characterization techniques, either *in situ* (synchrotron x-ray diffraction, Rutherford backscattering spectrometry, sheet resistance measurements…) or *ex situ* (Rutherford backscattering spectrometry, ion beam channelling, pole figure measurements, transmission electron microscopy…). In particular, the use of real-time techniques, i.e., investigating the phase formation and growth kinetics *during* the reaction, has shown to be particularly beneficial in order not to overlook any transient (but crucial) phases or amorphous phases (which escape detection with X-ray diffraction).

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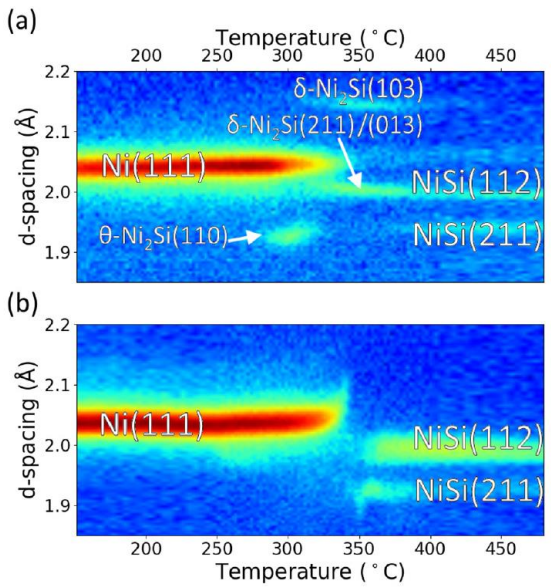

Figure 1: *In situ* XRD measurements of the reaction of a 35 nm Ni film on Si(100) for (a) an unimplanted sample and (b) a sample implanted with 1 × 10^{16} N cm^{-2} at 40 keV/atom. The absence of a diffraction peak in the temperature region between 330°C and 350°C for the implanted sample, originates from the formation of an amorphous Ni-Si layer.

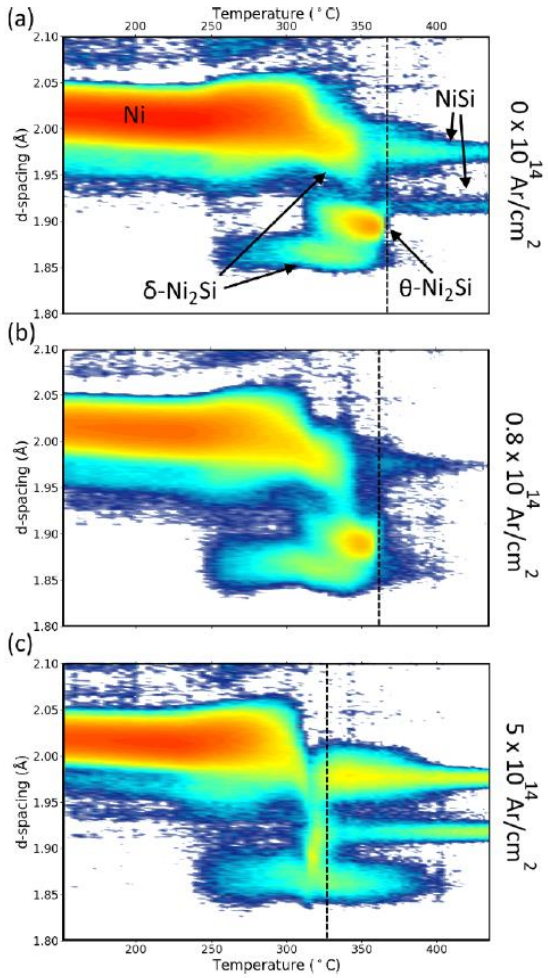

Figure 2: *In situ* XRD measurements of the reaction of a 13 nm Ni film on Si(100), for (a) an unimplanted sample, (b) a sample implanted with 0.8 × 10^{14} and (c) 5 × 10^{14} Ar cm^{-2} at 60 keV. The samples were annealed at a rate of 0.333°C/s. The silicide phases, as evidenced by their diffraction peaks, are indicated in (a). The dashed lines indicate the appearance of the NiSi phase, which occurs at lower temperature as the Ar concentration increases.

Material screening for future diffusion barriers: modelling of binary and ternary metal alloys and detailed experimental analysis of their barrier performance

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The exponential resistance increase in copper (Cu) interconnects due to densification and down scaling is a major challenge for future integrated circuits (ICs) [1]. Hence alternative copper diffusion barrier materials are necessary that replace the current TaN/Ta(Co) system [2,3].
In our work the diffusion behaviour of Cu into 7 binary and 3 ternary metal alloys with various compositions were investigated and compared. In order to achieve good diffusion barrier performance, the barrier material ideally has an amorphous structure, without grain boundaries that act as fast diffusion paths [4]. Therefore, the formation enthalpies of the alloys with various compositions were modelled using the Miedema model. With this semi-empirical model the stable amorphous composition range can be predicted [5,6]. Furthermore selected metal alloys were deposited via physical vapour deposition (PVD) on 300 mm wafers and their crystal structure, which was analysed by X-ray diffraction (XRD) analysis, was compared to the modelled data. Fig. 1 shows the results for one binary metal alloy (a) RuTa) and one ternary alloy (b) CoRuTa). The turquoise areas represent the theoretical amorphous composition range and the black dots and grids show the experimental XRD results. We can see that the black dots, which represent an amorphous structure lie all within those turquoise areas. Hence our model prediction works accurately. In addition to XRD analysis, the resistivity of the deposited alloys was measured via 4-point technique and the results are included in Fig. 1 in blue.

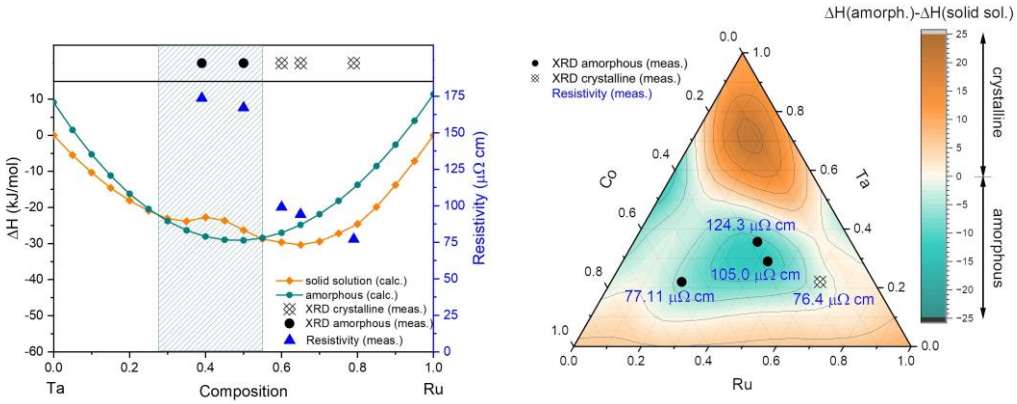

Fig. 1 Formation enthalpy for the solid solution and the amorphous phase calculated with the Miedema model, as well as crystallinity analyzed by XRD and resistivity (blue) for one binary metal alloy a) RuTa and one ternary metal alloy b) CoRuTa

After the theoretical and experimental evaluation, promising metal alloys were selected for the diffusion evaluation, which was performed by X-ray photoelectron spectroscopy (XPS) depth profiling. Therefore specifically designed material stacks were annealed at various temperatures for 10 minutes to induce copper diffusion. The XPS concentration profiles gave then insight into the diffusion mechanisms of Cu into those alloys. With this analysis we were able to categorize the diffusion behaviour and we found metal alloys with excellent barrier performance that could be alternatives to the currently used TaN.

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Contact Strategies for SiC Power Devices

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The necessity to reduce the environmental footprint of human activity, expressed in the Paris agreements in 2015 (COP21), is prompting governments to turn their attention to more respectful and responsible energy consumption. To achieve the reduction objectives of greenhouse gas emissions, key resolutions focus on improving the energy efficiency of electrical systems and the electrification of transportation. In this context, largely driven by Electrical Vehicle (EV) market, development of new semiconductors for power applications, that improve power efficiency compared to silicon, is a key issue. Today, Silicon Carbide (SiC) is the wide bandgap semiconductor, working under a high temperature and high power, that leads the market, with Gallium Nitride (GaN) as emerging competitor. Junction Bipolar Schottky (JBS) diodes and MOSFET transistors, that are the widespread elementary devices in any SiC-based power systems, are realized in the well-established 4H-SiC polytype and most of the famous brands embed in their EV these SiC-based power devices. To improve quality, reliability and efficiency of the power systems, contacts on SiC devices is one of the major milestones.

In this work, using a JBS diode as an ideal test vehicle, we will review both the Schottky and ohmic contacts used in 4H-SiC devices and the associated progresses. Recently, the new generations of 4H-SiC devices are fabricated on thinned wafers to significantly reduce substrate contribution to the R_{ON} in vertical topologies and improve their power efficiency. But the use of thinned wafers has a large impact on the device fabrication flow. Therefore, for vertical devices, the ohmic contact, that is classically fabricated using rapid thermal annealing (RTA), is no more a solution. In the last years, the device improvement, requiring fabrication modifications, has been carried out using laser thermal annealing (LTA). Indeed, LTA is mandatory to fabricate ohmic contact due to the low substrate temperature elevation that must be achieved in the process flow.

In the presentation, we will mainly focus on LTA advances for SiC vertical devices, going from the better understanding of ohmic contact by the means of TCAD simulations up to their physical characterization and electrical performance consecutive to laser irradiation [1–3].

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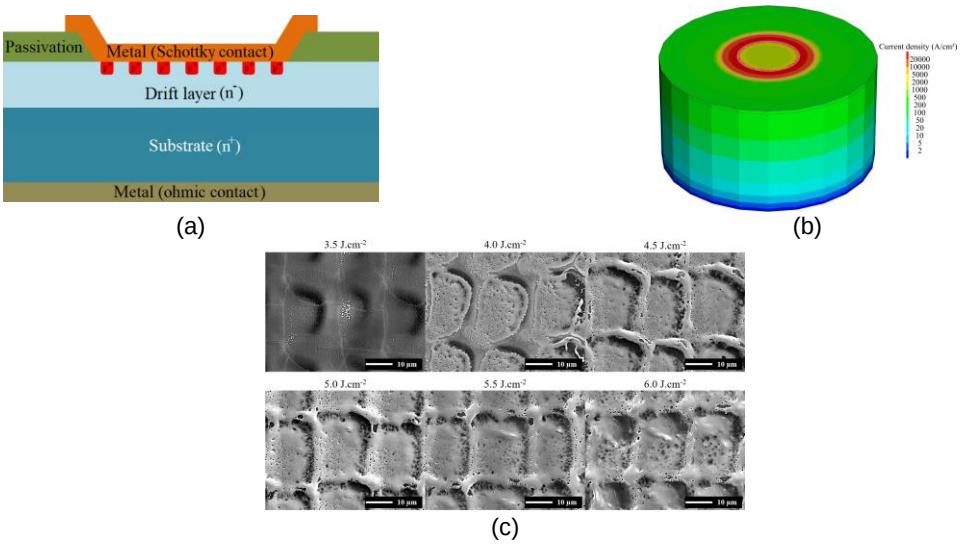

Fig. 1: (a) Example of 4H-SiC JBS structure, (b) 3D simulation of a c-TLM structure, (c) SEM images of Ni LTA annealed at fluences between 3.5 and 6.0 J cm^{-2}.

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Characterization and Modelling of C-doped buffers in GaN HEMTs

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GaN devices whether for RF or switching applications are undoubtedly the nowadays more promising devices for improving functionality and efficiency of modern electronic systems. The most adopted structure so far is the lateral HEMT one which combines both the high electric field strength property of the GaN material with the high mobility electron channels that can be formed at the AlGaN/GaN heterostructure.

Being a lateral structure and due to the need of withstanding large operating voltages, insulating layers are needed to prevent vertical and lateral conduction during off-state device operation. Carbon doped GaN buffer layers have been proved since their first adoption to be suited for achieving the device blocking capabilities required in power applications [1]. Nevertheless, their introduction within the device epitaxial structure also led to the onset of a limiting mechanism known as dynamic on-resistance (R_{ON}) degradation. Said phenomenon typically shows up when the device is rapidly switched on after biasing it into a high voltage off-state condition, resulting in an increase of the device R_{ON} and the onset of a time dependence, i.e. dynamic R_{ON}. This mechanism is quite detrimental for device operation since larger than expected R_{ON} values are severely impacting the operation of the device but also strongly undermining the expected improvement in efficiency due to the larger conduction losses related to the increased device R_{ON}.

An in-depth comprehension of the role of Carbon dopants within the device epitaxy thus became mandatory to understand its influence on device performance. In [2] the observed current decrease in carbon-doped GaN test structure during back gating measurements has been explained simply by means of a thermally activated hole-emission process with E_A=0.9 eV, which basically corresponds to the distance of the acceptor-like hole-trap level from the GaN valence band. The proposed hole-trap model basically relies on the emission of holes from acceptor traps which becomes then negatively ionized when a large voltage is applied in off-state conditions. When the device is then turned on, the negatively ionized acceptor creates a negative charge buildup within the buffer layer partially depleting the electron channel and thus increasing the R_{ON} values.

The adoption of the hole-traps model for explaining the electrical behaviour of Carbon-doped buffer layers has also allowed to understand several other phenomena observed during device R_{ON} characterization. The often observed dynamic-R_{ON} bell-shape degradation at the increase of the device drain voltage has been for example explained in [3]. With the aid of numerical simulations, it has been shown that at the increase of the drain voltage the R_{ON} degradation would be expected to increase if no other mechanisms, beside the hole-emission from the acceptor traps, would take place. At the increasing of device voltages though, electric field driven phenomena such as example impact ionization will become more likely to happen. Simulations showed that the onset of impact ionization leads to the formation of holes within the buffer region thus leading to a compensation mechanism of the negatively ionized acceptor traps with a consequent recovery in the electron channel density, i.e. a lowering of the device R_{ON} at the increase of the applied off-state drain voltage.

In conclusion, while still several aspects related to the Carbon-doping within the insulating layers need to be investigated, several ones have been understood thus helping the development and the improvement of device performances that has been experienced in the last years.

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Ohmic Contact Formation and Atomic Layer Processing for Nitride Devices

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Nitride devices e.g. AlGaN/GaN heterostructures are one of the main candidates for current power electronics and RF applications [1,2]. To improve device performance materials with either higher spontaneous polarization fields to increase carrier density in the two-dimensional electron gas (2DEG) formed at the heterointerface, or with a higher band gap are investigated [3, 4]. In both cases, the formation of the ohmic contact to the 2DEG is demanding and for the smaller and smaller devices the contact resistance of source and drain becomes crucial for the resulting ON-resistance. Here, our efforts to develop material stacks to form ohmic contacts with ultra-low contact resistance to the different heterostructures will be summarized. Varying the standard approach of a Ti/Al/Ni/Au contact stack V [5] and other transition metals were used to lower the thermal budget for alloy formation and gold free stacks like V/Al/Ti/TiN [6] were investigated to enable CMOS compatibility.
On the other hand, dielectric thin films are introduced by atomic layer deposition (ALD) to lower gate leakage current and hence increase the ON/OFF ratio further in a so-called MISHEMT (metal insulator semiconductor high electron mobility transistor) device. The impact of a fully amorphous dielectric (Al_2O_3), which was kept amorphous by the integration of a low thermal budget ohmic contact [5], was compared to an epitaxial dielectric film ($GdScO_3$) [7]. Due to the band alignment and the high dielectric constant of $GdScO_3$, the spillover effect as it was seen for Al_2O_3 [8] has been suppressed, and a reduction of threshold voltage shift due to the additional capacitance by the dielectric layer has been achieved. In addition, $AlTiO_x$ films were investigated as gate dielectrics, which enable a field and band alignment engineering allowing gate leakage reduction with minimal threshold voltage shift [9].
These approaches can be combined with atomic layer etching processes (ALE) to further reduce contact resistance by a source drain recess, and shift threshold voltage towards positive bias by a gate recess [10]. In the last case, a combination with *in-situ* ALD processes allows preventing an unwanted increase of gate leakage current by the recess process.

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Local substrate removal enabling next generation fully vertical GaN-on-Si power devices

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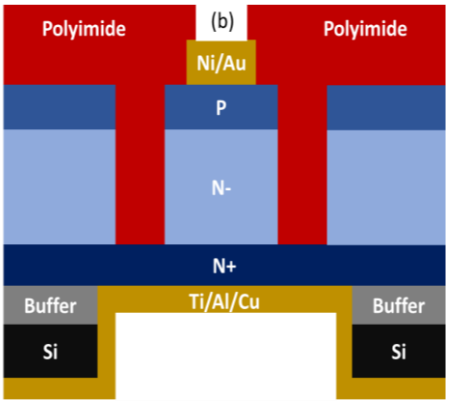
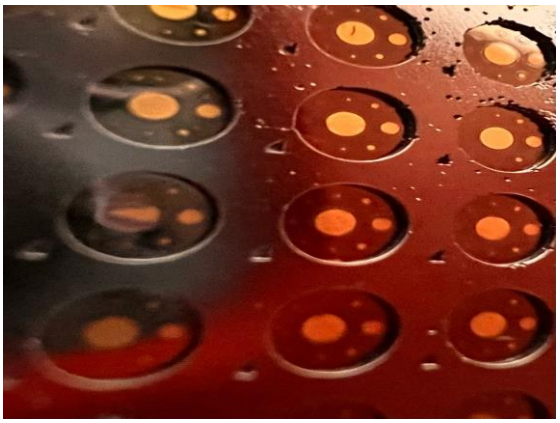
Although qualified up to 650 V voltage operation, lateral GaN devices are subject to severe limitations for higher voltage applications such as a large device size, surface trap related reliability concerns or the absence of avalanche breakdown due to the peak electric field at the gate vicinity. This led to the vertical GaN development, which is under extensive investigations worldwide as all the above-mentioned issues could be cured. State-of-the-art vertical GaN devices are fabricated on bulk GaN substrates, thanks to the high quality of the substrates in terms of low dislocation density and low impurity concentrations. However, they are prohibitively expensive, and only rather small area substrates are available.
In this talk, we will describe the current status of GaN-based fully vertical devices grown on large diameter silicon substrate. Despite the common belief about the limited drift layer thickness or wafer diameter due to the large mismatch in coefficient of thermal expansion (CTE) between Si and GaN, we will show that a local substrate removal with suitable related growth and process optimization enabled outstanding initial achievements such as extremely low on-resistance in kV-class fully vertical pn diodes with avalanche breakdown capability [1,2].



Schematic cross section of fully vertical GaN-on-Si pn diodes.



Backside view of pn diodes after Si and buffer removal

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Novel Trends in Interface Engineering for Wide Band Gap (SiC and GaN) power devices

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Nowadays, the world energy consumption is expected to grow by nearly 50% until 2050, with a 30% increase in the electricity demand in the next decade. Hence, in order to guarantee a sustainable future for our society, a better power management and a more efficient use of the energy have become mandatory. In this context, the development of new semiconductor technologies for power electronics, providing a better efficiency with respect to silicon (Si), is a key enabler for the sustainability transition. Wide band gap (WBG) semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), are the ideal choice for the next generation of efficient power electronic devices. In fact, they provide excellent physical and electronic properties, and better performances with respect to Si devices in terms of breakdown voltage, on-resistance, leakage current, maximum temperature operation, etc. [1,2]. Hence, SiC and GaN are gradually pervading strategic market sectors, in which high efficient components are required, e.g. consumer electronics, automotive, transportations, energy conversion in renewable energies, etc.

Diodes and transistors are elementary active components of all energy conversion systems in power electronics. In particular, SiC- and GaN-based discrete devices are already commercialized in a variety of products, including Schottky diodes, Junction Barrier Schottky (JBS) diodes, Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and High Electron Mobility Transistors (HEMTs) (see Fig. 1a). While today SiC and GaN devices have reached a notable technological maturity, leading to the replacement of the traditional Si power components in many applications, the need to push WBG semiconductors towards their ideal limits is currently the driving force for further technological breakthroughs [3]. In this context, metal/semiconductor and insulator/semiconductor interfaces are key parts, requiring to be accurately engineered to achieve the desired devices performances.

In this talk, some recent achievements of CNR-IMM group will be presented as case studies of novel interface engineering approaches to improve SiC and GaN unipolar devices performances.

Regarding 4H-SiC, a full control of the Schottky barrier height is a challenging issue, since the work function of common metals cannot be varied over a wide range. In addition, some of the commonly used metals (e.g. Ti, Ni) are extremely susceptible to react with SiC upon annealing. Hence, novel solutions based on refractory metallic compound are under investigation. In particular, the use of tungsten-based systems (e.g. WC) can be a promising solution to achieve low Φ_B values (lower than conventional Ti barrier) with a thermal stability up to 700°C [4] (see Fig. 1b). Moreover, it has been recently shown that a controlled reduction of the Schottky barrier height can be achieved also either through the local n-type heavy doping at the metal/SiC interface [5,6], as well as by non-conventional "sulfurization" surface treatments leading to Fermi level pinning effects [7].

In the case of 4H-SiC MOSFETs, nitridation processes in N_2O or NO of the SiO_2/SiC interfaces are commonly used to reduce the interface state density and, hence, increase the channel mobility. However, the presence of carbon-related defects due to interface re-oxidation effects can be detrimental for both the channel mobility and the device threshold voltage stability [8]. Hence, the fine control of the post-deposition annealing time is required to optimise the MOSFET interfacial transport and mitigate the threshold voltage instability [9]. In this context, the latest frontier in engineering the insulator/SiC interface in SiC MOSFET technology is the introduction of novel high-k dielectrics [10]. In this case, while Al_2O_3 is the most common investigated system, the notable charge trapping effects occurring in this system are preventing its practical use in SiC devices [11]. Hence, nanolaminated (Al_2O_3/HfO_2) [12] or stacked AlN/Al_2O_3 [13] systems have been proposed to overcome the limitations of single layers high-k, producing under appropriate condition epitaxial interfaces with promising electrical results.

On the other hand, AlGaN/GaN heterostructures grown on Si substrates are attracting the largest interest in the WBG community, owing to the perspectives of a large scale integration in Si-fabs. For this purpose, however, "Au-free" contact processes must be developed, in order to avoid contaminations and guarantee the CMOS compatibility [14]. Ti/Al/Ti and Ta/Al/Ta Au-free Ohmic contacts show low specific contact resistance ρ_c at 600°C, favoured by the formation of a TiN interface layer with a lower barrier Φ_B [15]. A further reduction of the annealing temperature and metal/AlGaN barrier has been recently achieved by inserting a thin Carbon interlayer at the Ti/AlGaN interface [16]

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(Fig. 1c). On the other hand, also a novel WC metallization has been considered as “Au-free” Schottky contact in AlGaN/GaN heterostructures [17], in alternative to the standard Ni/Au contacts.
Finally, the development of normally-off HEMTs is one of the most crucial challenges in GaN technology [18]. While normally-off p-GaN HEMTs are already commercialized, they still suffer from threshold voltage instability effects that can be associated to the defects generation upon gate bias stress [19]. In this technology, a correct prediction of the device lifetime can be reached only by taking into account the correct transport mechanisms at the metal gate / p-GaN interfaces [20]. As alternative approach, recessed gate hybrid MISHEMTs are currently under investigation in the GaN community. However, the choice of an appropriate gate insulator is still a critical issue in GaN technology. Al_2O_3 –based layers grown by ALD have been recently indicated as valid solution, despite the optimal processes to deal with metal/Al_2O_3/GaN structure is still under evaluation.

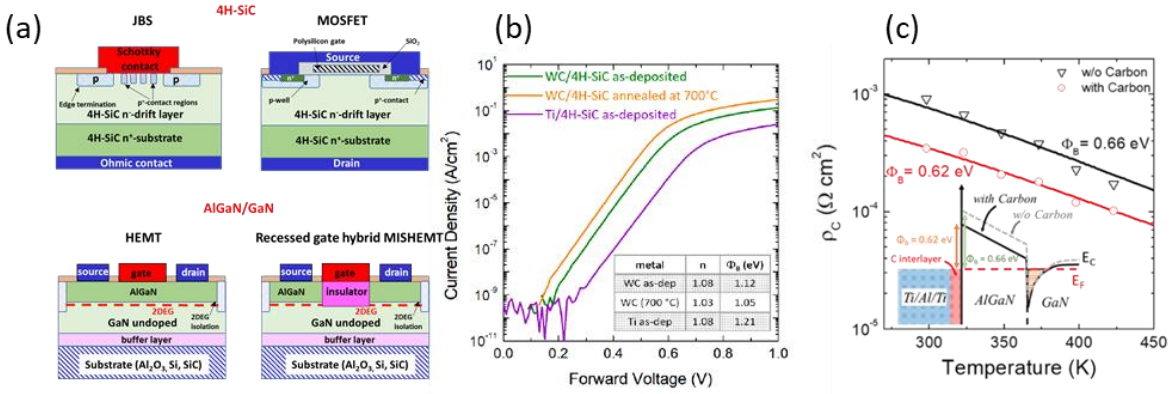

Fig. 1 (a): Examples of SiC and GaN devices. (b) Forward characteristics of 4H-SiC Schottky diodes with W and WC contacts, compared with the standard Ti metal. (c) Temperature-dependence of specific contact resistance ρ_c for Ti/Al/Ti contacts to AlGaN/GaN heterostructures without and with carbon interfacial layer.

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Silicon Carbide technologies for high demanding power applications

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STMicroelectronics

For several decades, the adoption of Silicon Carbide (SiC) as a wide band gap semiconductor in the microelectronic industry was limited due to technological issues such as low carrier mobility and inner defectivity, as well as preconceived notions about oxide structure robustness, lifetime reliability, operative degradation, and production yield.
Despite the fact that superior physical properties indicated SiC as a natural Si replacer in the power semiconductor field, it was not until the end of the last decade that ST, with a proactive approach, together with a visionary customer, demonstrated the advantages of introducing Silicon Carbide in demanding automotive applications such as traction inverter and on-board charger.
This was the starting point of an exciting journey that brought a revolution in power electronics. Efficiency is the key concept driving the transition from Si to SiC. Every stage of energy conversion, from energy generation to end-use application, needs to be optimized to improve efficiency, and can benefit from SiC adoption as a semiconductor including higher efficiency, higher power density, and higher temperature operation.
The next challenge for this journey is high-volume manufacturing capability to manage exponential demand growth, and ST is shaping manufacturing sites in Italy, Singapore, Morocco and China to maximize production and serve such impressive requests at their best. In the talk I will describe the technological competitive advantages of ST strategy in the SiC power field, including devices and packages, as well as product portfolio and marketing strategy.

Study of metal line patterning strategy for 300 mm superconducting BEOL

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Introduction:

The development of new Quantum technologies based on superconducting Qubits [1],[2] or spin Qubits[3], [4] becomes a major subject of interest for numerous applications in communication and data treatment. In this context, several approaches enable the fabrication of those devices [5],[6]. In this work a derivative method from VLSI device is chosen with the 28 nm FDSOI technology as a baseline. For this approach operating at low temperature, a superconducting rooting development becomes crucial especially for short distance connections with specific architectures (Fig 1).

Although superconducting material properties are the key targets, these layers also have to be easily integrated in an industrial process flow. Indeed, the selected materials, commonly used in microelectronics, must keep their superconducting properties for narrow lines down to a CD of 100 nm after etching, stripping, cleaning and CMP steps.

1 Superconducting characterisation on blanket wafers

Metallic layers material have been selected based on their critical temperature T_c (higher than 1 K) and their integration capabilities, which led us to consider TaN and TiN. The first step was to characterize their T_c on blanket wafers. All samples resistance versus temperature were measured down to 350 mK. In a previous work, the superconducting properties of a 40 nm thick PVD TaN film were improved by adjusting the N_2 flow during deposition to obtain specific phases [7]. This process development lead to an increase of the T_c up to 2,1 K compared to the standard process with a T_c of 1K (Fig 2). Some recent improvements resulted in a higher T_c of 2,6 K for the same thickness.

For the TiN, the resistance versus temperature is plotted for 3 layers from 10 nm to 40 nm thick and a critical temperature up to 3,6 K is achieved for the 40 nm layer (Fig 3). This is in good agreement with the state of the art [8]. The superconducting properties measured for both materials (TiN and TaN) are compatible with BEOL requirement for quantum application, we will then observe the influence of the patterning on the T_c.

2 Line patterns etching and characterisation

After TiN and TaN layer deposition, the lithography was performed on a 193nm stepper to reach 100 nm line critical dimension. Etching trials were carried out on a 300 mm industrial ICP chamber using Cl_2 chemistry with or without HBr or CH_4 addition. A parametric study of Cl_2 based chemistries was performed to evaluate such criteria as CD profile control, and selectivity between TaN and TiN. Optical Emission Spectroscopy (OES) and Xray Photo-electon Spectroscopy (XPS) were conducted in order to understand the etching mechanisms.

Regarding the TiN, straight profiles (around 85° of steepness) and good CD control (CD bias = 6 nm) are achieved with Cl_2/HBr chemistries but micro masking is observed (Fig 4). The micromasking phenomenon will be further discussed in terms of etching mechanisms. The use of CH_4 instead of HBr overcomes this issue while keeping a good profile (around 81° of steepness) with an etch rate of 70 nm/min (Fig 5). Regarding TaN, lower etch rates are observed in comparison with TiN which might be attributed to a higher Ta-N binding energy and lower by-product volatility (as example 60 nm/min versus 125 nm/min with Cl_2/Ar). A selectivity TiN:TaN of about 4.6 is achieved by adding CH_4 in the Cl_2 based chemistry with an etch rate of 70 nm/min for TiN and 18 nm/min for TaN. Interestingly, the steepness can be controlled from 74° with Cl_2/HBr (Fig 6) to 60° with pure BCl_3 by tuning the etching chemistry.

The T_c of TiN lines etched with Cl_2/CH_4 and TaN lines etched with Cl_2/Ar were measured. The results show only a minor decrease of T_c (-0.2 K) and a small ΔT increase of the TaN lines compared to the blanket results (Fig 7). However, the TiN lines exhibit multiple transitions (Fig 8), which might be explained by an inhomogeneity of the line. We will further discuss those unexpected T_c transitions.

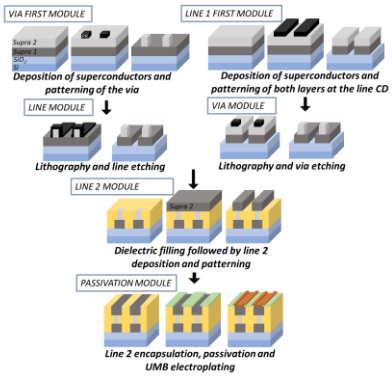

Figure 1 Patterning approach : Process Flow

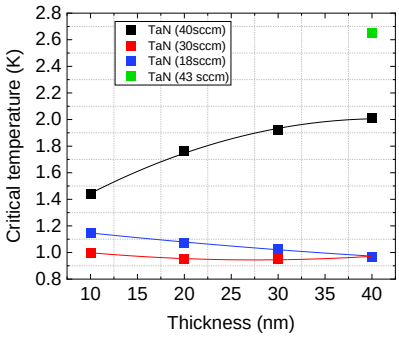

Figure 2 Critical temperature variation of TaN thin film versus thickness and Nitrogen flow, the lines are here to guide the eye

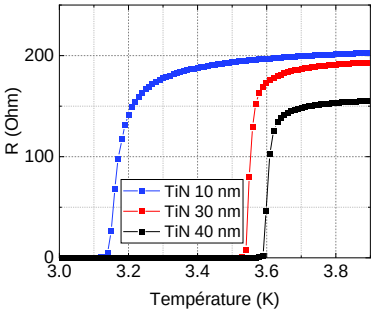

Figure 3 Resistance as a function of the temperature for TiN samples with thicknesses from 10 to 40 nm

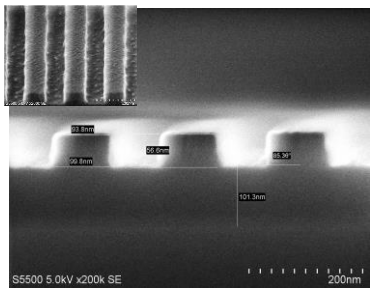

Figure 4 Cross section of 100 nm TiN lines etched with Cl_2/HBr

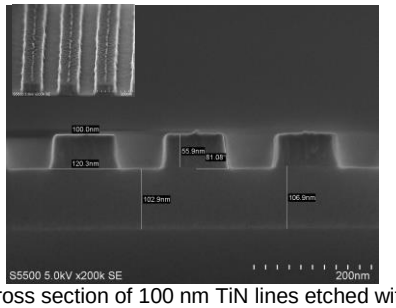

Figure 5 Cross section of 100 nm TiN lines etched with Cl_2/CH_4

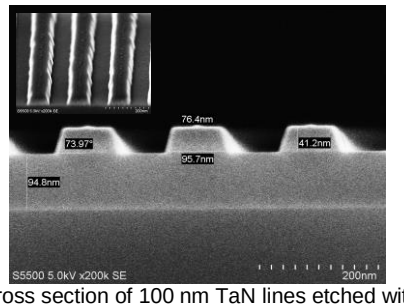

Figure 6 Cross section of 100 nm TaN lines etched with Cl2/HBr

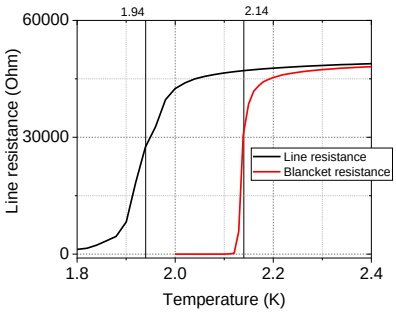

Figure 7 The resistance as a function of temperature for a 100 nm CD TaN line with a length of 60 µm and a blanket TaN layer with a thickness of 40 nm

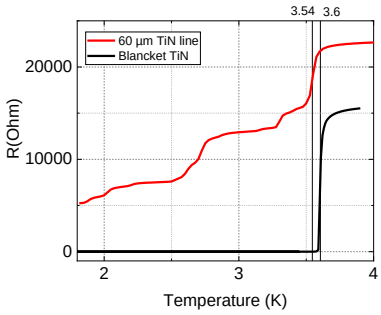

Figure 8 Resistance versus temperature of a CD 100 nm TiN line of 60 µm with a thickness of 40 nm and a blanket TiN layer

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ITO and NiO_x/ITO off-axis PVD deposition for transparent contact application

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ITO (Indium Tin Oxyde) is an optically transparent and electrically conductive material. It is mainly used as a spreading layer for optoeleconics devives such as LED, laser or µ-display. Concerning µ-display, blue and green native colors are obtained on GaN epitaxial layers. Even if N-type contact growth on these materials is well documented in the literature, obtaining a transparent P-type contact remains a key challenge to perform device integration and obtain best performances of µLED devices. Direct ITO deposition on the p-GaN surface is one way to obtain such P-type contact [1-3] whereas NiO_x / ITO bilayer stack seems a promising way to reach high-performance contact [1,4]. Present study will describe results obtained for both ITO and Ni/ITO deposition with an off-axis multiple-cathode Physical Vapor Deposition (PVD) chamber , Clover® on Endura™ 300mm platform from Applied Materials.

ITO deposition studies were performed on silicon 300mm wafer. Firstly, ITO films optoelectrical properties obtained by an ITO target, we will be described in regard with their deposition temperature, power supply and film thicknesses. For the last one the electro-optical properties are shown in Fig.1 and there is clearly an optimum thickness for the film best performances in the limit required by a transparent contact. In a second part, ITO compositions fine tuning through PVD co-sputtering will be addressed. Optical, electrical and chemical characterizations will be discussed to better understand the link between ITO composition and material performance.
Ni (x nm) / ITO (20 nm) bilayers were growth by PVD in Clover chamber. Annealing impact (atmosphere, temperature) on the bilayer's opto-electrical and depth composition were studied. Fig. 2 clearly shows that some conditions are favourable to obtain an NiO_x highly transparent interfacial layer between the ITO and the substrate. Concerning the Rs, high increase with O_2 annealing is observed whereas a very low increase under N_2 annealing and an improvement with Ar annealing are obtained.

Finally, TLM (Transfer Length Method) test-vehicle have been used to evaluate the specific contact resistivity of the p-type GaN / contact interface. Results obtained enabled to evaluate the link between ITO or bilayer composition and the electrical interface properties. Considering the material optical transmission, it allows to evaluate the best adapted process that could be used for a µ-LED device to improve his performances.

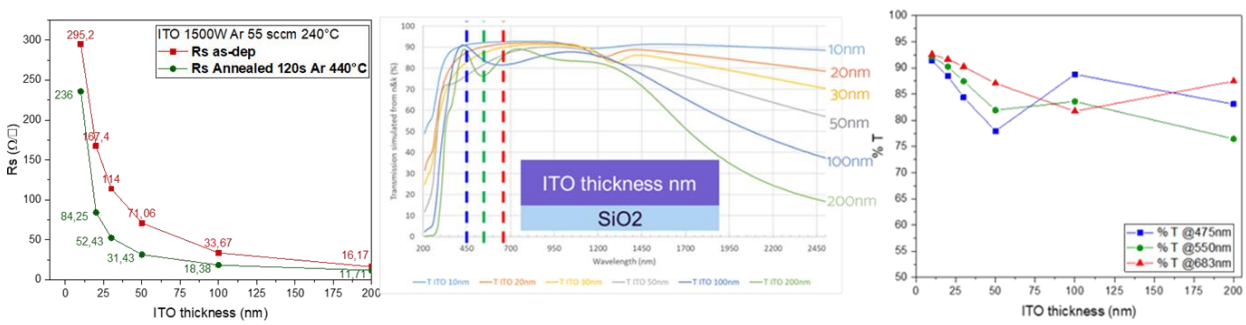

Figure 1: left: sheet resistance (Rs) values for different ITO thicknesses before and after annealing; right: optical transmission values vs ITO thickness, and summary of the values for blue / green / red light wavelengths.

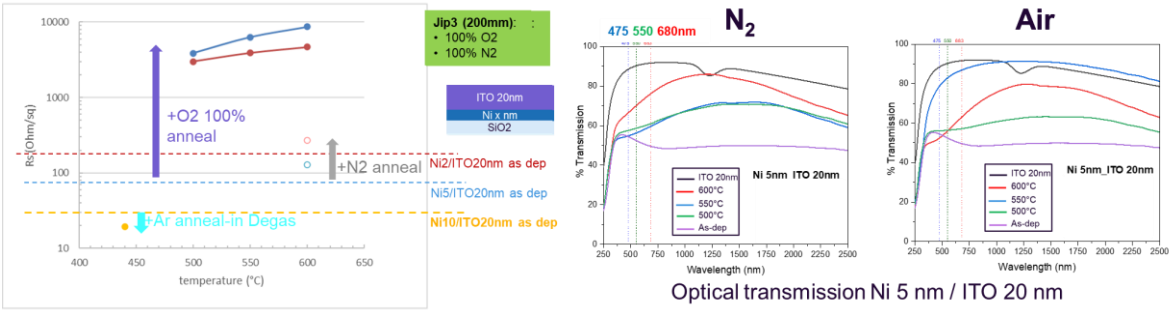

Figure 2: sheet resistance (Rs) variation and optical transmission for the Ni (x nm) / ITO (20 nm) bilayer as function of annealing atmosphere and temperature.

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Innovative correlative study based on NBD and EDS analyses for nanoscale characterizations of cobalt silicide film

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New RF technologies are being developed for various applications, including satellite, and automotive [1]. One of interesting options for 65 nm RF technology is to integrate an innovative Co silicide process. In the past decades, the development of 65 nm node dealt with the replacement of Co disilicide by Ni mono-silicide integrations [2]. The change was motivated by two main problems relative to Co silicide formation: the narrow-line effect and the Co disilicide formation temperature [2]. In that way, new approaches have been studied to form Co disilicide in small dimensions by introducing between the Co layer and Si substrate a Ti interlayer. Such process is known as TIME for Ti Interlayer-Mediated Epitaxy [3]. Indeed, the targeted microstructure for Co silicide layer generates an hetero-epitaxy with the Si(100) substrate, what could be an enabler for Co disilicide films in critical dimensions. This ternary system is complex to integrate in microelectronics but reveals clear challenges in terms of characterizations.

To investigate the influence of TIME process on the final Co-silicide microstructure, several samples were prepared. A stack formed of Ti, Co and TiN layers is deposited by PVD (Physical Vapor Deposition). The samples will be referred as A, B and C dealing with the subsequent deposition thicknesses for each layer: A Ti 5 nm/Co 7.2 nm/ TiN 10nm, B and C are identical: Ti 3nm/Co 7.2nm/ TiN 10nm. The annealing temperatures will be different from those 3 layers. The standard silicide process flow starts with a first anneal at 500 °C for 30 s, and a second anneal at 800 °C for 20 s to form the less-resistive $CoSi_2$ phase.

In this study, the primary objective is to observe the influence of titanium during the silicidation process and evaluate the presence of any identified parasitic phases like CoTi, TiSi, and Ti. To achieve these goals, EDS (Energy Dispersive X-ray Diffraction Spectroscopy) and NBD (NanoBeam diffraction) TEM techniques are combined to investigate the local microstructure in detail. TEM- EDS is used to validate the stoichiometry of the sample using cliff and lorimer quantification [4]. NBD, with Automated Crystal Orientation and Phase Mappings (ACOM-TEM) [5], uses electron diffraction to study phases presence and crystalline orientation at a nanometer scale. Diffraction analysis is performed using the NanoMEGAS ASTAR system implemented on a JEOL NeoARM TEM with 1.5 nm step size resolution.

The STEM-HAADF images comparison shows the impact of the couple thickness/temperature on silicidation (fig 1). As the films grow thicker the layers are more homogeneous. The correlation of those HAADF maps with elemental EDS maps (fig.2) enables to highlight the presence of titanium inside CoSi grains. The quantification of different regions on those samples with or without titanium is summarized in table 1. The quantification results on the three samples A indicate a stoichiometry close to $CoSi_2$ structure. These results information will be implemented on further crystal orientation analysis.

Figure 3 shows the virtual bright field image and the orientation map for the 3 samples. The indexing of diffraction patterns mainly revealed the presence of the $CoSi_2$ phase for all 3 samples. This phase corresponds to a face-centered cubic phase with lattice parameters close to those of the Si substrate phase. Therefore, the orientation mapping overestimates the presence of $CoSi_2$ in the substrate. Moreover, the orientation map correlated with the $CoSi_2$ index map point out the presence of 2 preferential orientations. One is along the (001) plane, which is the growth plane of Si, and the second is along the (-122) plane. Finally, the titanium inclusions do not affect the crystal structure of the different cobalt silicides, and thus, no CoTi or TiSix grains were detected. The NBD analysis also did not reveal the presence of residual cobalt grains. To summarize, a simple TEM-EDS analysis is not sufficient to deeply study such a complex silicidation process. But its combination with NBD allows for a more in-depth analysis for the detection of phases and the organization of the silicide matrix in the presence of a thin initial Ti layer. The alliance of both technique enables to get complete sets of characterization allowing to better understand complex material implemented in microelectronics applications.

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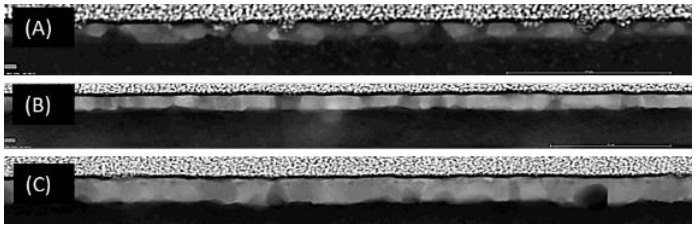

Figure 1: STEM HAADF images of $CoSi_x$ layers for (A), (B) and (C).

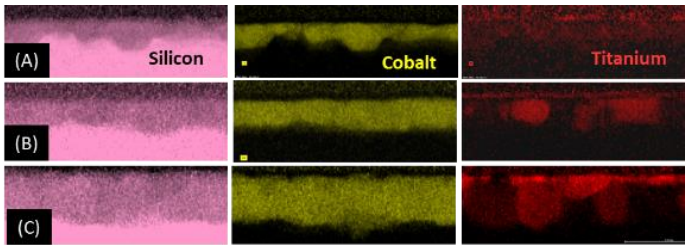

Figure 2: EDS quantified maps of $CoSi_x$ layers of samples (A),(B) and (C)

	Sample A		Sample B		Sample C	
Co	35 at.%	/	25 at.%	23 at.%	35 at.%	29 at.%
Si	64 at .%	/	74 at.%	67 at.%	64 at.%	60 at.%
Ti	>1 at.%	/	1 at%	10%	1 at.%	11 at.%

Table 1: EDS quantification on different area of the 3 samples without or with Titanium content

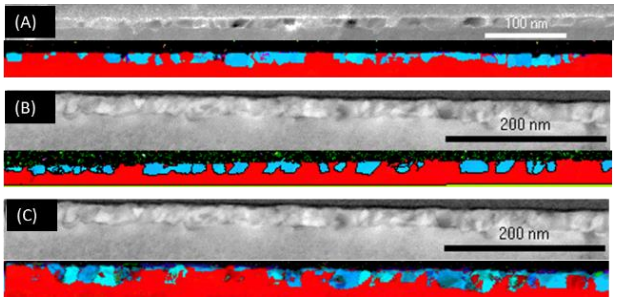

Figure 3: Virtual Bright Field and NBD orientation maps for $CoSi_2$ indexation phase for samples (A), (B) and (C)

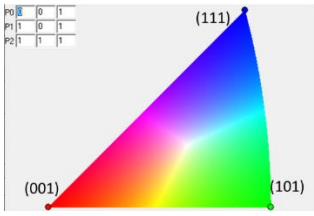

Figure 4: Index map of $CoSi_2$ cubic phase

Innovative approaches on TiSi-based contact development for µTrench IGBT technology: C54-$TiSi_2$ to TiSi phase transition

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In the frame of power technologies development, new Isolated Gate Bipolar Transistor (IGBT) technology uses large W plugs realized through a micro trench (µTRC) approach. In IGBT devices is fundamental to short circuit the p-type implanted region, known as body, with n-type implanted region, called source (Fig. 1a and Fig. 1b). When the holes travel from the body region and create a large enough forward bias voltage at junction J1 (Fig. 1a), the parasitic n-p-n transistor could be turned on. In this case the IGBT works as a thyristor, the gate loses control on the current leading to device destruction by excessive power dissipation. To avoid this destructive phenomenon, contact resistance with body and source must be minimized.
Ti based silicide has been widely used to provide an ohmic contact to the active Si regions. Ti/TiN bilayer, usually used as diffusion barrier inside W contacts, has been employed as a reactive metal layer to form titanium silicide-based contacts [1,2]. Two well-known stable phases of Ti based silicide are C49-$TiSi_2$ and C54-$TiSi_2$. With this respect, the estimated intrinsic resistivity for TiSi phase is three times higher than the C49-$TiSi_2$ one (around 60 µΩ.cm) and twelve times higher than the C54-$TiSi_2$ phase (around 15 µΩ.cm) on blanket wafers [1].
With planar contacts where silicide formation is provided only on bottom-contact surface, specific process integration aimed to obtain C54-$TiSi_2$ phase is widely used, since it guarantees a stable low resistive phase [3]. This integration includes: contact etch patterning, pre-deposition cleaning, deposition of Ti/TiN by-layer and rapid thermal annealing (RTA) to provide Ti-Si reaction. The same integration sequence was initially used on µTRC-IGBT, which aims to realize a 3D structure with an ohmic contact both on bottom and walls of the contact. This solution generated a C54-$TiSi_2$ on µTRC bottom (Fig 2a, 2b, 2c, 2e, 2f and 3a) with low contact resistance on p-type doped silicon in body region (noted as RC_P-). However, the same solution generated high resistive interface on µTRC walls with n-type doped silicon in source region (noted RC_N+ for resistance contact on N+). Since the widely used PVD Ti is a low conformal deposition, a trial was made to increase the nominal Ti deposition thickness in order to favor a thicker Ti layer on µTRC walls. This change led to the formation of a low resistive interface with source, low RC_N+, but a dramatic increase of contact resistance measured at the bottom, i.e. high RC_P- (Fig. 4). This phenomenon is expected to be due to an excessive formation of C54-TiSi2 on the planar surface at the bottom inducing barrier cracks and depletion of p-type species during silicidation process. This might be due to the Si diffusion to Ti/Si interface and the changes induced in the junction profile.
This paper concludes that µTRC-IGBT contacts development mainly deals with a change of C54-TiSi2 to TiSi phase transition: forming TiSi phase at the µTRC bottom (Fig 2g, 2h, 2i, 2j, 2k, 2l and 3b) with a low temperature RTA, we were both able to increase the Ti deposition rate on µTRC without generating an excess of silicide on bottom (Fig 4). In fact, TiSi crystalline phase presents a lower volume with respect to TiSi2 species, avoiding contact barrier cracks and p-type junction depletion on µTRC bottom.
To achieve the "3D-TiSi contacts" optimal integration, a Design of Experiment (DOE) approach was used to tackle morphological and electrical requirements, by varying the following process factors: contact pre-deposition cleaning, Ti PVD thickness, TiN thickness, RTA time and temperature. Methodology, DOE factors and robustness, silicide characterization and electrical results will be deeply discussed in the final paper.

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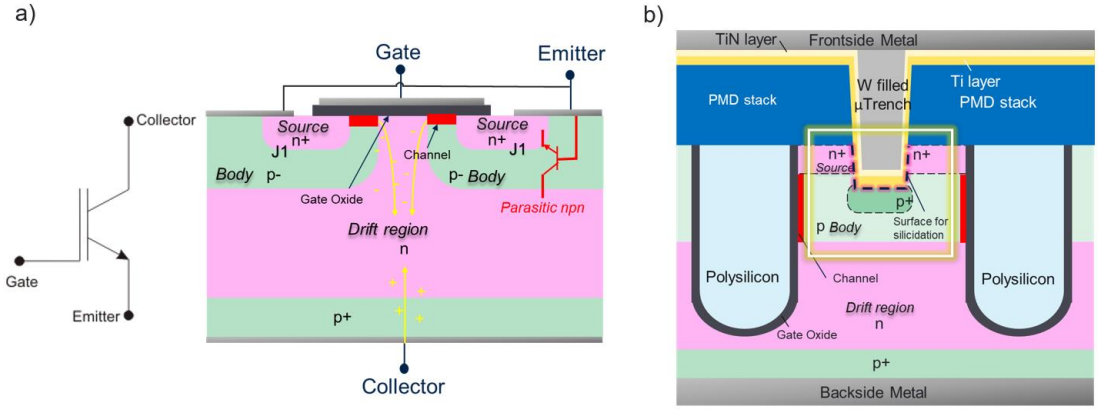

Figure 1: a) Electrical model of IGBT MOSFET presenting a wide base PNP transistor and connections between n+ and p- regions near the emitter; b)Schematic representations of W micro-trench inside IGBT devices to highlight the specific need for this technology of a "3D TiSi" formation to connect source and the body.

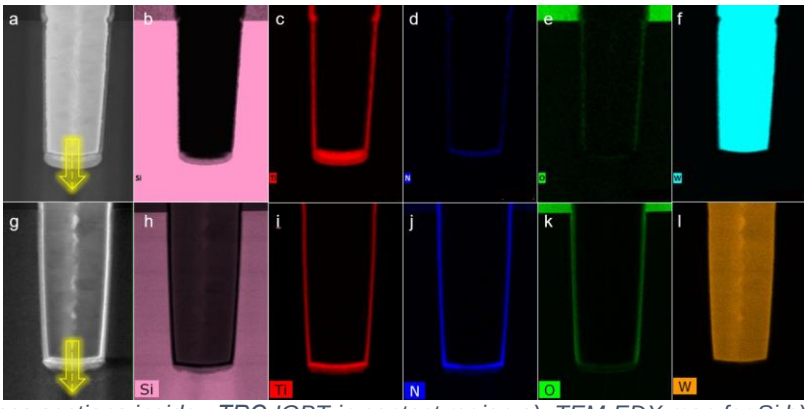

Figure 2: TEM cross sections inside µTRC-IGBT in contact region a), TEM-EDX map for Si b), Ti c), N d), O e), W f) related to $TiSi_2$ process flow; TEM cross sections inside µTRC-IGBT in contact region g), TEM-EDX map for Si h), Ti i), N j), O k), W l) related to the new TiSi process flow.

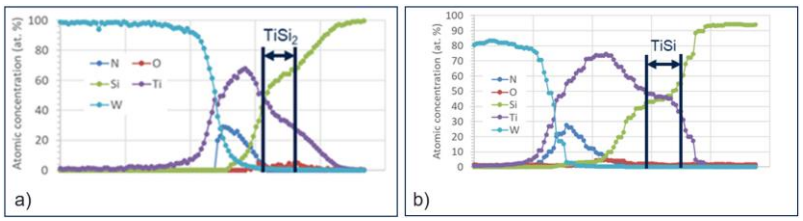

Figure 3: EDX profiles across the yellow array designed in Fig.2a a) and Fig.2g b).

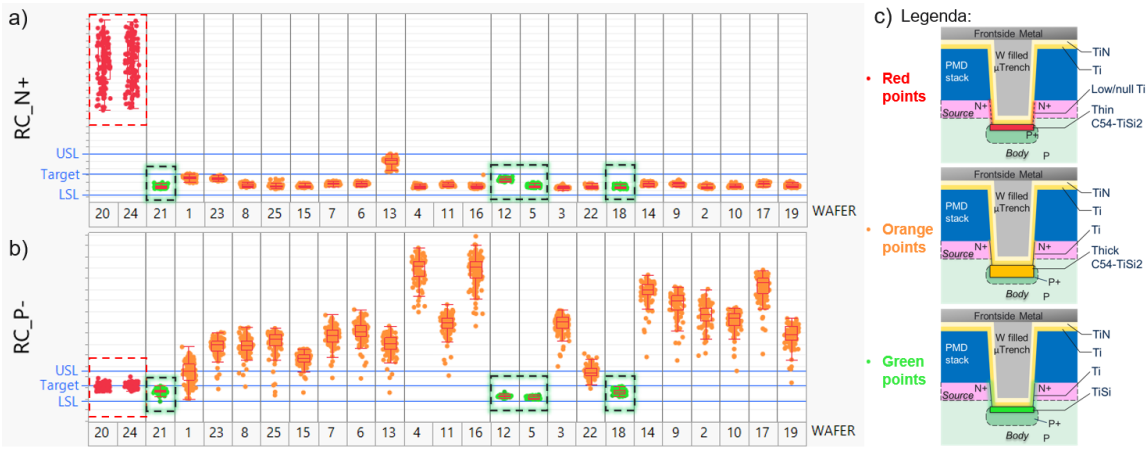

Figure 4: Contact resistance between µTRC walls and source (RC_N+) as a function of electrical DOE conditions a); contact resistance between µTRC bottom and body (RC_P-) as a function of electrical DOE conditions b); schematic representations of µTRC inside IGBT with "3D silicide" morphology as a function of electrical DOE conditions c).

Atomic Layer Deposition of Cobalt at Low Temperatures

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The conformal deposition of cobalt is still an ongoing topic of research. Applications are manyfold and include interconnects[1], seed layers for electroplating[2], magnetic sensor systems[3], and antibacterial coatings[4]. The thermal budget during film deposition is a crucial parameter which has to be taken into account. Here we present the development of a low temperature Atomic Layer Deposition (ALD) process for the formation of metallic cobalt thin films.

The professorship of Inorganic Chemistry at the Chemnitz University of Technology developed a set of cobalt precursors on the base of dicobalt-hexacarbonyl-alkynes as $[Co_2(CO)_6(RC{\equiv}CR')]$.[5] We evaluated a set of these precursors for chemical deposition methos using density functional theory (DFT) calculations. According to these calculations the precursor $[Co_2(CO)_6((CH_3)_3SiC{\equiv}CSi(CH_3)_3)]$ is the most favourable precursor for Chemical Vapour Deposition (CVD) as it thermally decomposes completely on the substrate surface. In contrast, precursor $[Co_2(CO)_6(HC{\equiv}CC_5H_{11})]$ was identified as the most favourable precursor for deposition via ALD as it adsorbs with adjected ($HC{\equiv}CC_5H_{11}$) group which can be easily removed by use of mobile hydrogen. A simplified scheme for the surface reaction and release of the hydrocarbon group is shown in Figure 1.

We developed an ALD process based on the DFT results by use of $[Co_2(CO)_6(HC{\equiv}CC_5H_{11})]$ as the cobalt precursor and hydrogen plasma.[6] The process development was done on a *scia Atol 200* reactor, which was designed and fabricated by *scia systems GmbH* in cooperation with *Fraunhofer ENAS* and the *Chemnitz University of Technology*. The processes took place on standardised 200 mm Si wafers with a preliminary SiO_2 layer of 100 nm thickness. The precursor was evaporated via bubbling method. A full ALD cycle consists of cobalt precursor pulse, Ar purge, H_2 plasma pulse, and a second Ar purge.

The deposited cobalt films were analysed by *in-vacuo* ellipsometry to determine in-line the film growth rates. Figure 2 shows the deposition rates in the temperature range from 35 °C to 125 °C showing the ALD window for this process within the range of 50 °C to 110 °C. *Ex-situ* measurements with spectroscopic ellipsometry were done to determine the thin film homogeneity on wafer level using a spiral measurement pattern with 5 mm edge exclusion. The optimised process had a film thickness deviation of about 1.5% relative standard deviation.
Additional measurements with X-ray photoelectron spectroscopy confirmed that the deposited films consist of cobalt in metallic state. Sole contaminations were identified as oxygen and carbon which are expected as the wafers were measured *ex situ* and may oxidise during transport.

Funding
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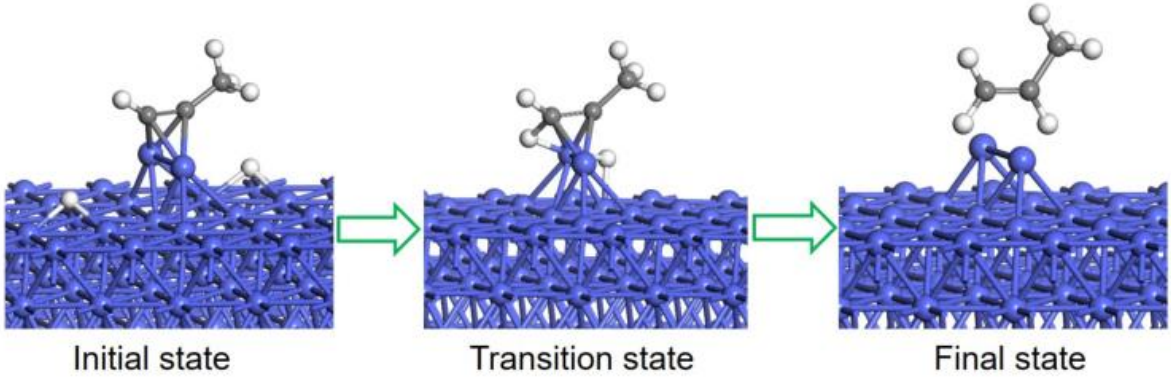

Figure 1: density functional theory simulations showing the surface reactions between hydrocarbon ligand and hydrogen.

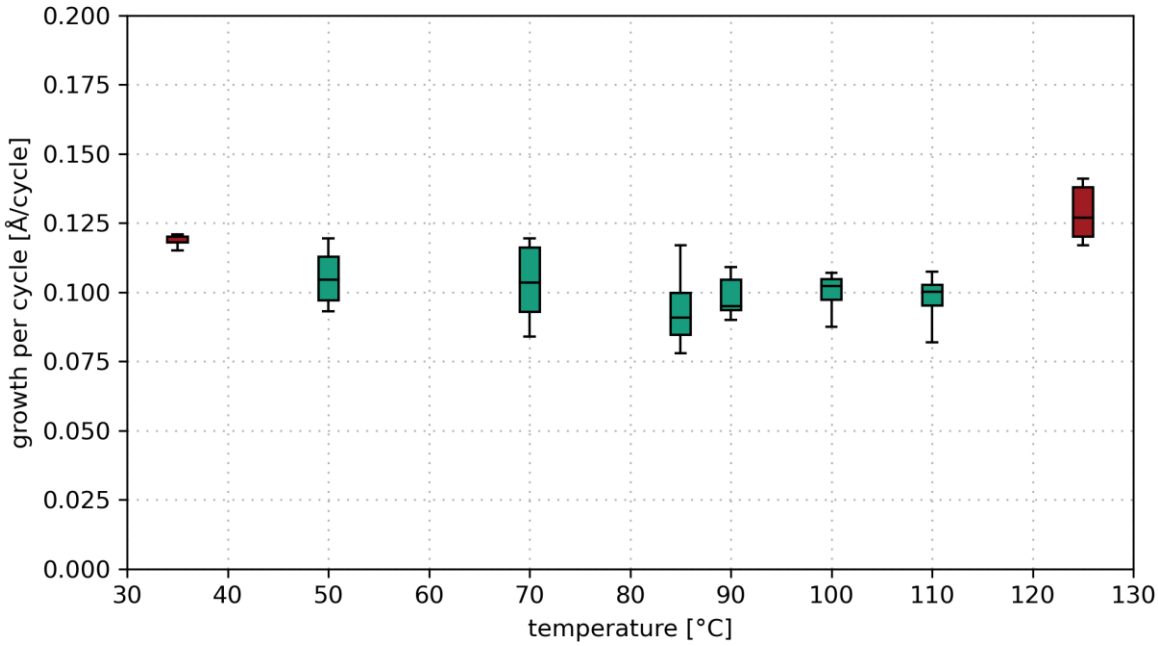

Figure 2: Temperature dependence of growth rate.

Silicidation of Next Generation of FD-SOI Devices: Effect of P Doping Level in epitaxial Si:P Films

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For the next generation of Fully Depleted Silicon On Insulator (FD-SOI) and Complementary Metal Oxide Semiconductor (CMOS) devices, advanced epitaxial processes with in-situ P-doped Si layers (for nMOS) have been developed to achieve ultra-low Raised Source and Drain (RSD) access resistance [1]. To date, Ni(Pt)-based silicides have been the reference contacts for FD-SOI devices. The doping process, i.e. ion implantation vs. in-situ, is known to affect the silicidation process [2]. For in-situ doped samples, phosphorus segregation was observed at the NiPt surface, and at the NiPt/Ni_2Si and Ni_2Si/Si interfaces after RTA1, but also at the NiSi surface and at the NiSi/Si interface after DSA2. In addition, the total NiSi thickness was measured to be thinner when formed on the in-situ doped silicon [3]. In this work, we study NiPt-based silicidation on 2 generations of Si:P epitaxy.

30 nm thick Si:P films were grown by epitaxy in a 300 mm RP-CVD chamber. Two generations of epitaxy with different doping levels were investigated. Gen #A results in low doped Si:P epilayers with a phosphorus content of about 0.3%, while Gen #B is a high doped Si:P epilayer with about 4% P. After cleaning in HF 0.5% solution followed by in-situ Siconi process, metallization of these Si:P films was performed using $Ni_{0.9}Pt_{0.1}$ metal (7 nm) capped with 7 nm TiN deposited using magnetron sputtering RF-PVD chambers. The wafers were then annealed by Rapid Thermal Annealing (RTA) processes at temperatures ranging from 200 to 450 °C for 20 s under an N_2 atmosphere. Finally, the samples were treated with hot sulfuric peroxide mixture solution to remove unreacted metals. We characterized the samples using four-point probe (sheet resistance measurements, R_{sh}), X-ray reflectivity (XRR), X-ray diffraction (XRD), and time-of-flight secondary ion mass spectrometry (TOF-SIMS) analyses.

Figure 1 shows the sheet resistance as a function of annealing temperature after selective etching (SE). At low temperatures, a shift in R_{sh} values between high and low doped Si:P samples is observed. This may be due to the different P content in the SiP layers. Between 200 °C and 250 °C, we see an increase in resistance for both samples. Between 250 °C and 300 °C, low-doped samples show a drop in resistivity (from 80 to 27 ohm/sq), while high-doped samples remain stable around 65 ohm/sq. The drop for the highly doped samples is observed between 300 °C and 350 °C. This R_{sh} evolution corresponds to the transition from the Ni-rich phase to NiSi. A plateau is reached at 20 ohm/sq, at 350 °C for low-doped and 400 °C for high-doped layers. This difference in behavior may be due to different levels of phosphorus. As observed by M. Lemang et al., the phosphorus could reduce the nickel diffusion rate because nickel and phosphorus could use the same diffusion pathways. These results are consistent with previous work by [4]. To confirm the phase change from the R_{sh} measurements, in-situ XRD was performed from room temperature to 500 °C with a 5 °C step (Figure 2). It shows the presence of NiPt and TiN in the XRD diagrams from room temperature to 150 °C. By increasing the temperature, the signal of NiPt disappears and the signal of NiSi appears at 250 °C for low-doped sample. The NiSi phase appears at a higher temperature, 350 °C, for the highly doped samples. This is in good correlation with the R_{sh} results, showing that the high P content delays the formation of the monosilicide. To investigate the distribution of phosphorus and its role in the phase change delay, samples were analyzed by TOF-SIMS. The SIMS profile of the low-doped sample annealed at 350 °C is shown in Figure 3. We observed phosphorus segregation at the NiSi/Si interface. This behavior is similar to that presented in [3], reinforcing the role of P as a retarder of the NiSi phase transformation.
By combining different characterization methods, we observed discrepancies between the silicidation of the 2 generations of Si:P epitaxy. We will discuss this further during the conference.

This work was supported by a grant from the French government, managed by the “Agence Nationale de la Recherche” under the France 2030 program: ANR-22-NEXG-0001 (NextGen project). The authors would like to thank Mickael Sanchez for his assistance and Sophie Guillemin for fruitful discussions.

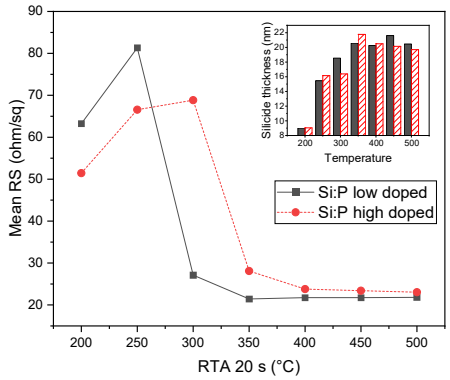

Figure 1: Sheet resistance evolution as a function of RTA temperature after selective etching.The inset shows the evolution of the silicide thickness measured by XRR with RTA temperature.

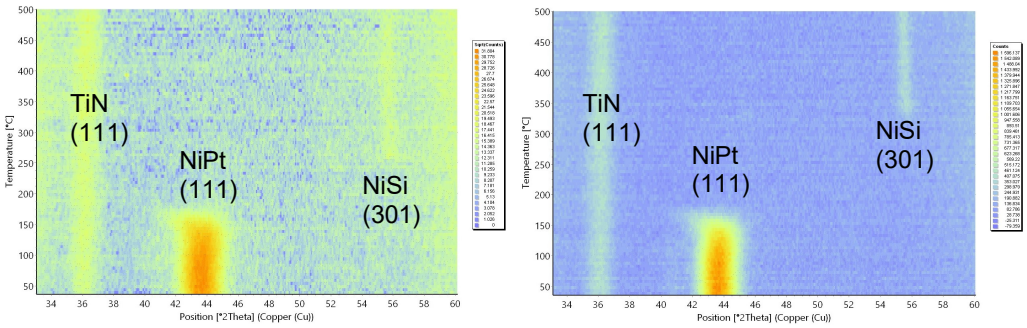

Figure 2: In-situ XRD θ-2θ diagrams during the annealing of a 7nm TiN + 7nm $Ni_{0.9}Pt_{0.1}$ film deposited on a phosphorus Si:P Gen#A (left) and Si:P Gen#B doped epitaxial layer (right).

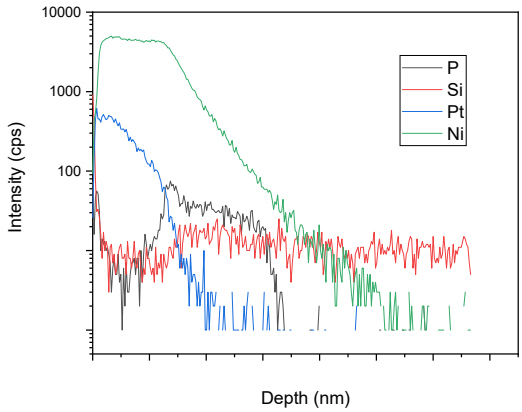

Figure 3: TOF-SIMS analysis of the NiPtSi / Si:P Gen#A stack annealed at 350°C for 20 s in N_2 and after selective etching.

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Multi-step Siconi pre-clean advantages for Ni(Pt)Si film formation in the frame of advanced FDSOI technology development

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The demand for microcontrollers in automotive market will continue to grow in the future, and for such applications, embedded Non-Volatile Memories (eNVM) have been raised as major devices [1]. Emerging Phase Change Memories (PCM), based on HK-metal-gate 28 nm FDSOI technology (Fig.1), is one of the best candidates to achieve these challenging requirements (noted FDSOI for Fully Depleted Silicon On Isolator). For this technology, Ni-based silicide is used as contacts on active Si regions (such as gate, source, and drain), due to its low resistivity, low thermal budget, and low silicon consumption during silicide formation [2]. Nevertheless, 28 nm FDSOI technology deals with three remaining challenges: 1) ultra-thin Ni(Pt)Si film formation presenting a final thickness, around 10 nm, due to the very thin Si layer on the top of embedded oxide; 2) A specific surface preparation scheme due to the high sensitivity to Sulfuric Peroxide Mixture (SPM, as H_2SO_4 in addition of H_2O_2 solutions) chemistry of metal gate stack, formed mainly by TiN layer ([3], Fig. 2); 3) Complex Ni(Pt)Si formation in small dimensions linked to a perfect Si surface preparation to avoid any remaining oxide before NiPt deposition. For the last ten years, in-situ remote plasma clean, called Siconi, becomes the standard surface preparation process for Ni-based integrations [4]. As described in Fig. 3, Siconi pre-clean is based on two main steps, called etch and anneal steps. During the etch step, the fluorosilicate salts are generated on the wafer through the reaction of NH_4F reactive species with SiO_2 thin film in presence (Fig. 3a). The sublimation of $(NH4)_2SiF_6$ salts is obtained by moving up the Si wafer near the showerhead maintained at 180 °C (Fig. 3b). Such fluorosilicate salts are quite volatile, and then transformed in SiF_4 and NH_3 gazes at 100 °C. Several previous works, mainly on TiSi advanced contacts, reported the interest for aggressive dimensions of a multistep Siconi process [5], [6]. Such process could play a role on the etching of oxide and nitride layers around gates, and then the opening of a “way” to SPM chemistry to spread up to the metal gate layer (Fig. 2). In this context, several SiCoNi pre-cleans have been investigated to improve Ni(Pt)Si thin film formation in small dimensions without damaging HK-metal gate structures. In this paper, we propose to review two separate studies performed on 300 mm blanket wafers. For the first one, complete Salicide process flow has been provided contrary to the second one for which characterizations were carried out just after NiPt layer deposition. For both, two types of SiCoNi pre-cleans have been studied as a single and multiple-step Siconi processes.

As a first result, significant reduction of Ni(Pt)Si thickness non-uniformity is measured by ellipsometry on the whole 300 mm wafer in the case of a double Siconi process, prior NiPt/TiN deposition (Fig. 4). Such improvement might be related to the fluorine species concentration at the Si surface before NiPt deposition, around 3 at. % as measured by XPS (not shown here). To clarify this point, ToF-SIMS and TEM-EELS characterizations were launched after NiPt deposition only for different Siconi pre-clean conditions. For all samples, an intermixing layer with a NiSi composition is formed at the NiPt/Si interface, and the thickness of this amorphous layer is measured by TEM near 3 nm- (Figs. 5a, b and c). Inside the intermixing layer, as shown on Figs.5 d, e and f), fluorine distribution is very different in the case of a single-step Siconi process versus a multiple one. A double peak could be easily identified for single step process contrary to the other. In Figs. 5 g, h and i), while fluorine content is below the detection limit for EELS experiment, focusing on nickel ionization edge might enable to overcome this problem by probing nickel chemical environment such as fluorine or oxygen. EELS spectra, acquired at nickel ionization edge, fine structures indicate chemical shifts between the several layers since Ni is bonded to Pt in NiPt film, and to Si in the intermixing layer (Fig. 5a as an example). Moreover, EELS spectra exhibit the typical fine structure of Ni bonded to Pt in NiPt layer for all SiCoNi processes. Regarding the NiSi intermixing layers, EELS fine structure changes due to new bonds with Si atoms but remains the same in the NiSi layer. However, for the multiple-step SiCoNi process, EELS fine structure evidences a double peak at the interface of NiSi and Si layers (in red, in Fig. 5h). This double peak indicates a new bonding and could be related to fluorine environment. Consequently, EELS study points out a specific Ni-F binding localized at the NiSi/Si interface for the multiple-step Siconi process. Deep analyses and discussions will be then proposed in the final paper to understand which mechanisms are involved during silicide surface preparation to explain the presented results based on morphological and chemical characterizations.

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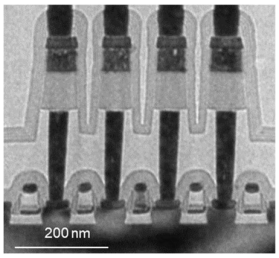

Fig. 1: TEM-cross sections of advanced low area phase change based on non-volatile memory (ePCM) realized with 28 nm FDSOI technology.

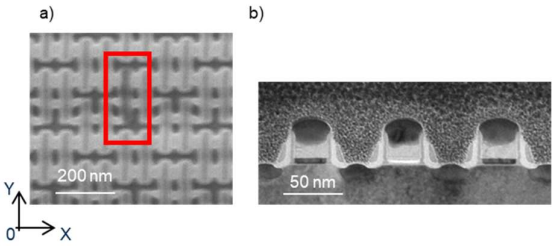

Fig. 2: Top-view SEM in SRAM arrays of a “black gate” a) defined as a TiN metal gate layer missing due to SPM chemistry etching during Ni(Pt)Si formation, as shown in b) on TEM cross-sections inside this defect.

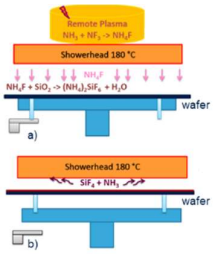

Fig. 3: Schematics of Siconi process including two main steps as $(NH4)_2SiF_6$ salts generation (etch) a) and their sublimation (anneal) at 100 °C on the top of the wafer b).

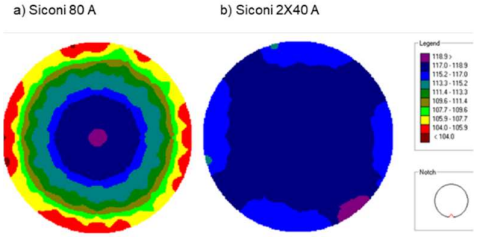

Fig. 4: Ni(Pt)Si film thickness measured by ellipsometry after RTA2 on 300 mm blanket wafers obtained after a single-step a) and multistep Siconi process b).

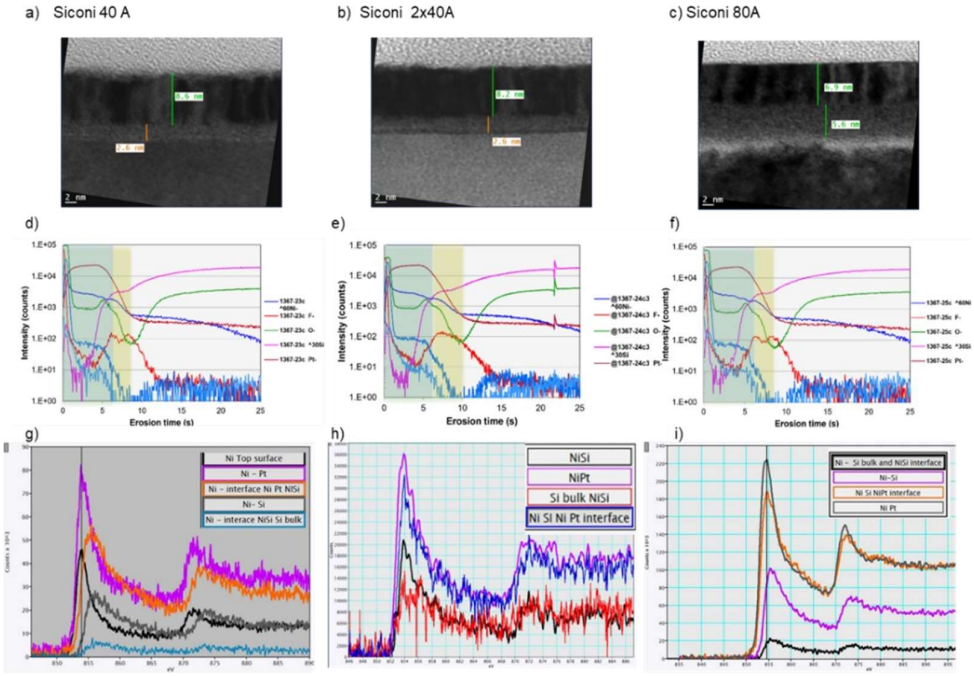

Fig. 5: TEM cross sections obtained after NiPt deposition provided after three different Siconi processes as Siconi 40 Å a), 2x40 Å b) and 80 Å c). ToF-SIMS profiles of Ni, Si, Pt, O and F elements for similar samples (d to f),and finally EELS spectra of nickel $L_{2,3}$ ionization edge, extracted from line profiles at different regions: interfaces between the NiPt/NiSi/Si bulk and in the core of each layer (g to i).

Chip Package Interaction assessment of WLCSP process steps by 3D FEM Thermo-mechanical simulation

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New power technologies are increasingly moving to Wafer Level Chip Scale Package (WLCSP) solutions [1], in order to optimize electrical connections, avoid parasitic loss and reduce overall size of the product. The integration of these package families, from a Chip Package Interaction (CPI) point of view, is very different from what has been already done and known on standard plastic packages: no thermo-mechanical stress due to wire bonding and molding compound is here present. Anyway, a risk assessment of WLCSP process must be addressed to study assembly impact on passivation and top metallization morphologies, due to the temperatures used to complete all the steps.
Finite Element Method (FEM) simulation is a powerful tool for evaluating stress due to thermal and mechanical mismatch, able to highlight worst conditions for different layout configurations.
In this work, a 3D WLCSP thermo-mechanical modeling activity is presented to evaluate stress generation during assembly phase. The interconnection system considered is a fan-in WLCSP with two organic insulator layers (PI1 and PI2), one redistribution metallic layer (RDL), under bump metallization (UBM) and solder balls. All these steps, excluding soldering, are performed at wafer level in an assembly fab. The silicon technology under investigation has a top metal scheme composed by a thick Al metal covered by two dielectrics: a Silicon Oxide and a final Silicon Nitride passivation film that is the material under analysis for this stress evaluation activity. A scheme of the package and die considered system is reported in Figure *1*.
Thermo-mechanical simulations are performed using Comsol Multiphysics software by a linear elastic materials model including initial stress of some layers if applicable. Silicon Nitride has been analysed considering its risk of breakage, so the considered physical quantity is the First Principal Stress.
Firstly, passivation stress has been analysed for different process steps: a comparison of stress at wafer level before assembly (simulation of a thermal treatment), after PI1 and PI2 curing, bumping and soldering is reported. PI2 curing appears as the most critical step: the simultaneous expansion of PI1, RDL and PI2 layers generates a high stress level in SiN passivation as reported in Figure *2*. Once identified the worst process step in terms of stress, also a comparison of different layout configurations is reported, considering different cases of RDL and PI2 opening.
Finally, some considerations about passivation breakage risk highlighted by this analysis and a way to design dedicated experimental trials are reported as conclusions and important outputs of this work.

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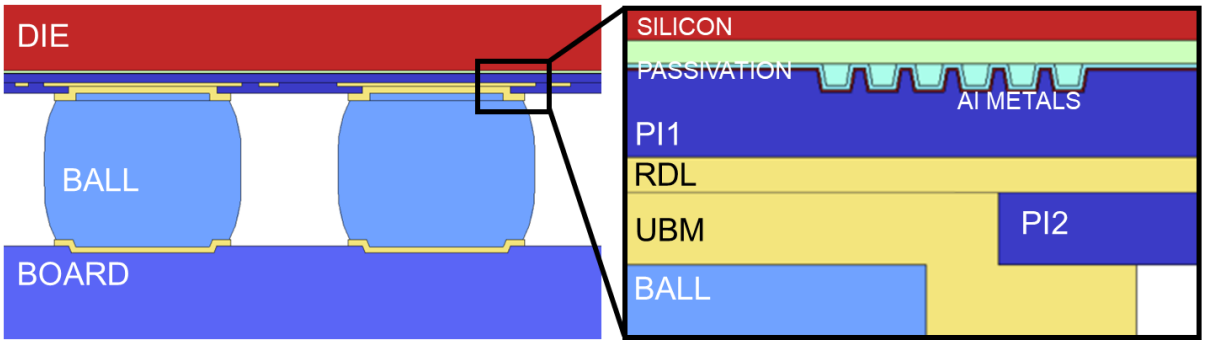

Figure 1. Cross section of a WLCSP FANIN package system; two layers of PI and one RDL is present on top of a die with Al final metallizations. UBM is present on both sides to allow ball soldering on die and on application board.

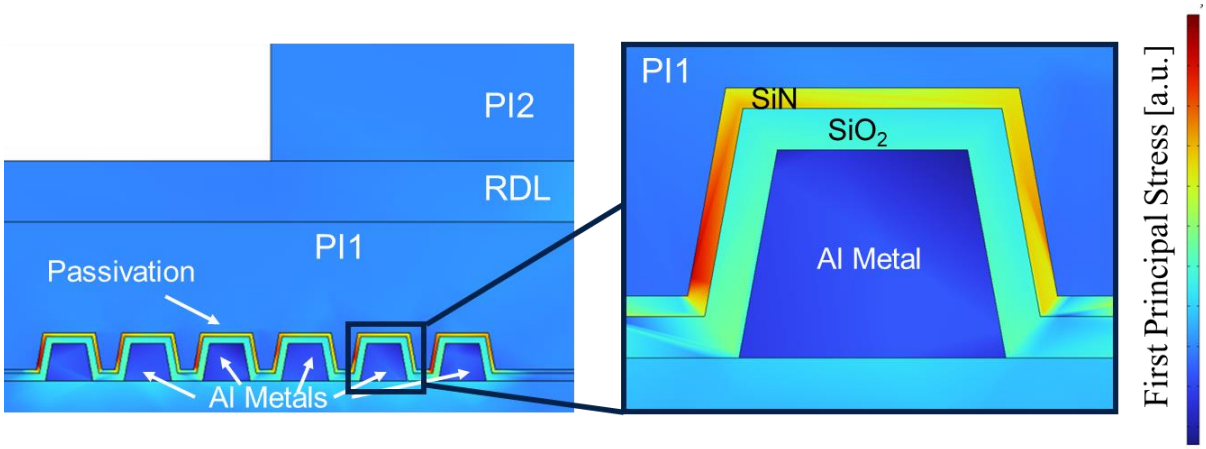

Figure 2. First Principal Stress at PI2 curing temperature; high stress found in SiN passivation layer.

Development of Novel Selective Barrier Metal for Low Via Resistance in Cu Damascene

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As the logic device node gets smaller, the impact of the resistance and capacitance (RC) time delays in the Back-End-of-Line (BEOL) interconnect becomes a significant factor in determining the performance of the chip. To minimize RC delay, it is crucial to focus on reducing the resistance in vias [1]. However, developing a barrier metal capable of maintaining barrier properties and withstanding severe stress at the bottom of vias in an extremely small metal pitch poses significant challenges. While Atomic Layer Deposition (ALD) Barrier Metal (BM) has been introduced to replace traditional Physical Vapor Deposition (PVD) BM to reduce via resistance [2], overcoming delamination issues due to stress build-up on the via bottom remains challenging, given ALD BM's impurity characteristics and stress differential from PVD BM.

This paper presents an optimized selective ALD barrier metal process designed to reduce via resistance while addressing the shortcomings of ALD BM. The selective deposition ALD process incorporates a concept where the deposition and removal process of self-assembled monolayers (SAM) is added to the existing copper (Cu) process [3-4] (Fig. 1). Before depositing the tantalum nitride (TaN) BM, SAM is selectively deposited on the exposed metal layer's surface, rather than the low-k Inter-Metal Dielectric (IMD) surface, providing hydrophobicity to prevent TaN deposition at the bottom of via during atomic layer deposition. Consequently, ALD TaN can be selectively deposited on the low-k surface, resulting in reduction of via resistance (15~20%) (Fig. 2). To achieve an effective selective deposition process, various factors such as SAM soaking time and temperature, ALD TaN thickness, plasma process for SAM removal, and physical vapor deposition conditions for densification must be considered. Optimizing SAM process conditions involves determining the deposition temperature and soaking time, ensuring SAM removal is easy. The optimal condition is derived based on the final ALD TaN film quality characteristics. The SAM removal process utilizes mild H2 plasma, selected to minimize plasma damage to IMD and meet the standard for completely removing carbon residue originated from SAM deposition (Fig. 3).

One of the most challenging issues in reducing via resistance is the reliability limitations, including stress migration and electro-migration in the copper damascene structure as the pitch decreases. Despite the trade-off between lower via resistance and reliable processes due to increased barrier metal thickness, ALD TaN barrier shows limitations in achieving better performance (Fig. 4). In this regard, selective ALD BM offers advantages in overcoming the limitations of ALD BM. This is attributed to the characteristics of Physical Vapor Deposition (PVD) Barrier Metal (BM), where even with a thinner BM thickness, maintenance at the bottom of via and improved adhesion properties at the sidewalls of via can be achieved. This advantage is evident in stress simulation results and improved health-of-line (HOL) in the wide metal stack chain Test Element Group (TEG), as depicted in Figure 5. Furthermore, excellent yield results were obtained by optimizing the subsequent PVD BM treatment process conditions (Fig. 5).

In conclusion, to reduce via resistance of the copper (Cu) interconnect, we performed process optimization for Self-Assembled Monolayers (SAM) deposition and removal conditions which are critical parameters in the selective Atomic Layer Deposition (ALD) BM process. The via resistance was successfully reduced by 20% or more. Additionally, addressing delamination and reliability issues arising from stress concentration in the tiny pitch structure is a challenging aspect of Barrier Metal (BM) scaling. However, through the optimization of selective ALD BM, these challenges can be addressed by reducing impurities at via bottom and enhancing film density at the sidewalls of the via.

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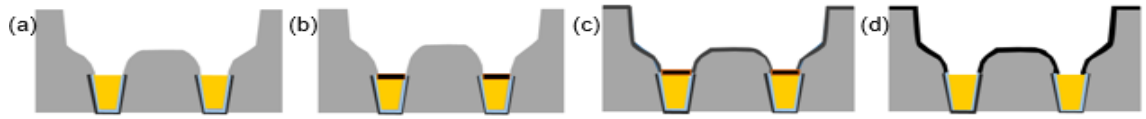

Fig. 1. Process sequence of selective ALD TaN Deposition (a) after pre-clean for interface (b) SAM deposition (c) selective ALD TaN deposition (d) SAM removal process

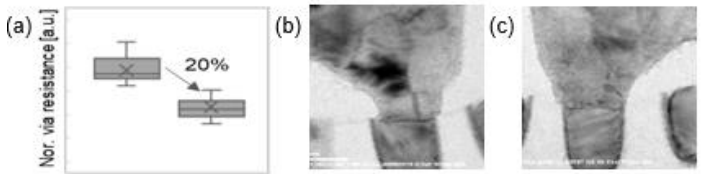

Fig. 2. (a) Via Resistance gain of selective BM (b) TEM image of ALD BM
(c) TEM image of Selective BM

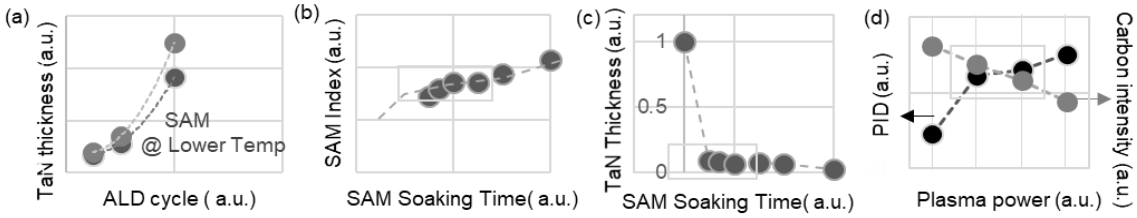

Fig. 3. Optimization of selective BM (a) SAM temp vs. TaN thickness (b) SAM soaking time vs SAM thickness (c) SAM soaking time vs. TaN thickness (d) PID (plasma induced damage for LK vs. intensity of carbon impurity by Plasma power for SAM removal

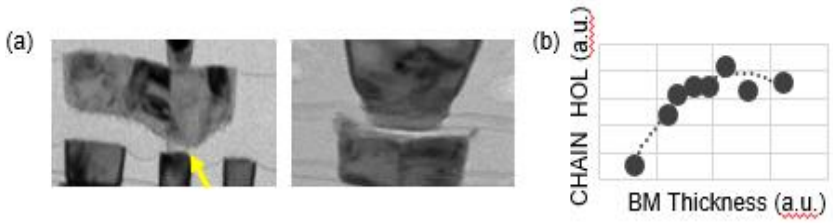

Fig. 4. (a) ALD BM delamination issue at via bottom
(b) BM thickness vs. Via Chain HOL (health of line, %)

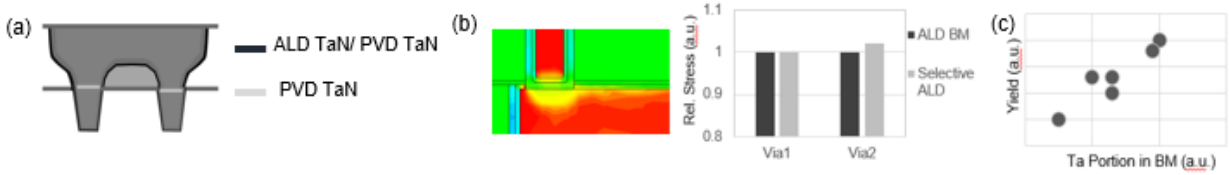

Fig. 5. (a) Selective ALD BM final BM profile: PVD BM only at via bottom
(b) Stress simulation of ALD BM (c) Ta portion in BM vs. Yield

Proposal Ultrafast Soldering of the BGA package for Carbon Neutrality

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Carbon neutrality in the manufacturing of electronics requires the net zero commitment by 2050. Green peace warns that the semiconductor industry's power consumption will more than double by 2030. According to Mackensey report, the share of CO2 gas in the semiconductor industry consists of 20% of law materials, 35% of gas and 45% of electrical power. Semiconductor industry equipment has very high standby current compared to other industries. The convection reflow process is a typical soldering technique, but it is known that soldering SAC 305 consumes 29.5 kWh of energy.

For example, the mobile phone is assembled by more than 1000 elements such as actives devices and passive devices. In addition, electronic packages are becoming more compact for higher density and performance, making reliable interconnection between different devices a major problem.

In general, the assembly process between different devices for electronics has been applied to a reflow process by using IR base energy.

Also, carbon neutral policies have begun to require minimization of the energy used by electronic products. For example, minimizing the energy required for manufacturing electronic products can be attempted in various ways such as recycling of used materials, reducing the number of manufacturing processes, reducing the process temperature, etc.

However, conventional IR base reflow processes require process temperatures higher than the melting point and long process times of at least 300 seconds. Also, the reflow process cause problems with advanced package such as chip delamination and warpage problems in soldering interconnections. On the other hand, Laser-assisted bonding (LAB) has been highlighted as an advanced soldering interconnection process because of an ultrafast bonding process and thermal selectivity. However, the laser energy can be applied to solder process for local joint or point soldering. Because the IPL soldering process is 1/10th shorter than reflow soldering, the IPL soldering process reduces warpage issues in packaged components and thermal damage to polymer components.

Reliability of package was evaluated by using shear test method and drop impact test method.

Furthermore, the thickness of intermetallic compound (IMC) formed at the interface of the COG package by IPL soldering was 4-5 times thinner than that of conventional reflow process. As a whole, bonding strength of the BGA package by IPL soldering was 3 times higher that of reflow process. Drop impact strength of the BGA package by IPL soldering was 4 times higher than conventional reflow. The Crack of the BGA component assembled on OSP surface finished PCB substrate were mainly propagated along the layer of Cu6Sn5.

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Formation by nonlinear reactive diffusion of the amorphous Ni silicide upon rapid thermal anneals

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Silicides are used in microelectronics devices as contacts and for technology nodes below 65 nm, the Ni silicide is the preferred material because of its low resistivity as well as the low thermal budget and low Si consumption [1]. Pt has been added to the Ni silicide to limit the detrimental agglomeration issue that becomes more stringent when the silicide thickness is decreased to follow the devices downscaling in microelectronics. The addition fo Pt changes the silicide formation but the kinetics and mechanisms related to these changes have not been deeply investigated. In particular, the kinetics of formation of the first silicide is of great importance when a partial silicidation is performed during the silicide process since it allows to precisely control the final thickness of the contact. Indeed, in the self-aligned silicide process (salicide) with partial silicidation, a given thickness of first silicide is formed during the first rapid thermal anneal (RTA) by selecting the thermal budget and, after selective etch of the unreacted metal, is converted in NiSi with the desired thickness during the second rapid thermal anneal. In this work, the growth kinetics of the first silicide is investigated in detail and a new model considering nonlinear diffusion is proposed for the growth law. The influence of a pre-amorphization implant (PAI) on the first phase kinetics is also investigated.

10 nm $Ni_{0.9}Pt_{0.1}$ layers covered by 7 nm thick TiN capping layer were deposited without vacuum breaking by magnetron sputtering after the substrate cleaning. Rapid thermal anneals (RTA) for five different times at temperatures ranging from 200 to 230°C were then performed in order to keep the reaction partial. The unreacted NiPt and TiN layers were finally removed by wet selective etching for the determination of the silicide thickness by X-ray reflectivity (XRR) with a precision of ± 0.1 nm. TEM analysis coupled with EDX (Electron Dispersive X-Ray) spectroscopy were also performed.

TEM analysis show that the first silicide is an amorphous silicide with a composition ranging between 33 and 45 at.% of Si. A TTT diagram is used to point out the influence of the RTAs on the growth of the amorphous silicide by inhibition of the silicide's crystallization.
The growth kinetics of this amorphous silicide during RTA type annealing was determined by XRR measurements of the silicide thickness (Fig. 1). To determine the growth law, the linear parabolic model is first considered but non-physical parameters were obtained for all samples and all temperatures (Fig. 2). A nonlinear reactive diffusion model in which the growth rate is proportional to the hyperbolic sinus of the gradient of chemical potential is developed to accurately reproduce the experimental results (Fig. 3). This behaviour is attributed to the nanometric thicknesses (< 18 nm) of the amorphous silicide that lead to strong gradient of driving force (chemical potential).
From this model, the effective diffusion coefficient as well as its activation energy were determined for the three samples with PAI and the reference sample without PAI. The differences in effective diffusion coefficients (and activation energy) provide some understanding of the PAI influence on the growth kinetics of the silicidation process. The influence of the substrate amorphization on the silicide growth is discussed : the Ge PAI has an accelerating effect on the silicide formation that could be related to thermodynamic (driving force) but also kinetics (self-diffusion coefficient). However, the Ge+C PAI seems to cancel the influence of the Ge PAI. The validity and applicability of the nonlinear reactive diffusion, considering the application for microelectronics contacts, are also discussed.

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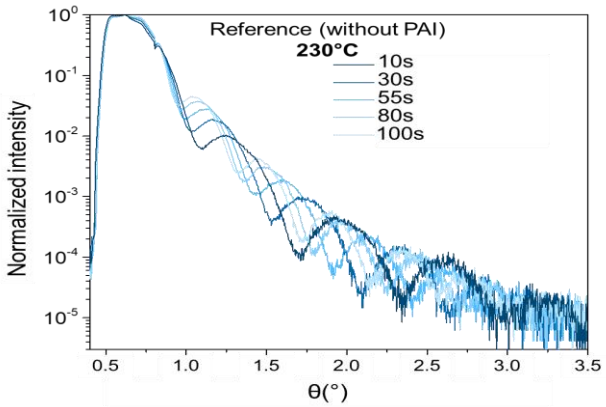

Fig. 1 : X-ray reflectivity curves (XRR) for the reference samples having undergone a thermal budget of 230°C for 10, 30, 55, 80 and 100 seconds.

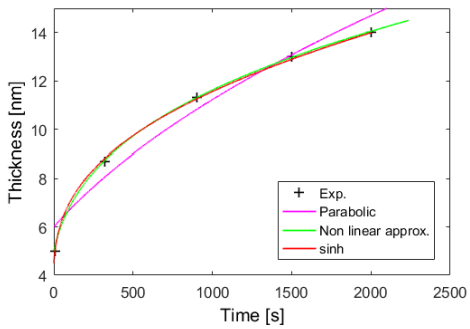

Fig. 2 : Fit of the experimental thickness for RTA annealing at 200°C of the reference sample using nonlinear reactive diffusion law (Eq. 1), parabolic law (Eq.2) and an approximation of the nonlinear law. The symbols represent experimental values.

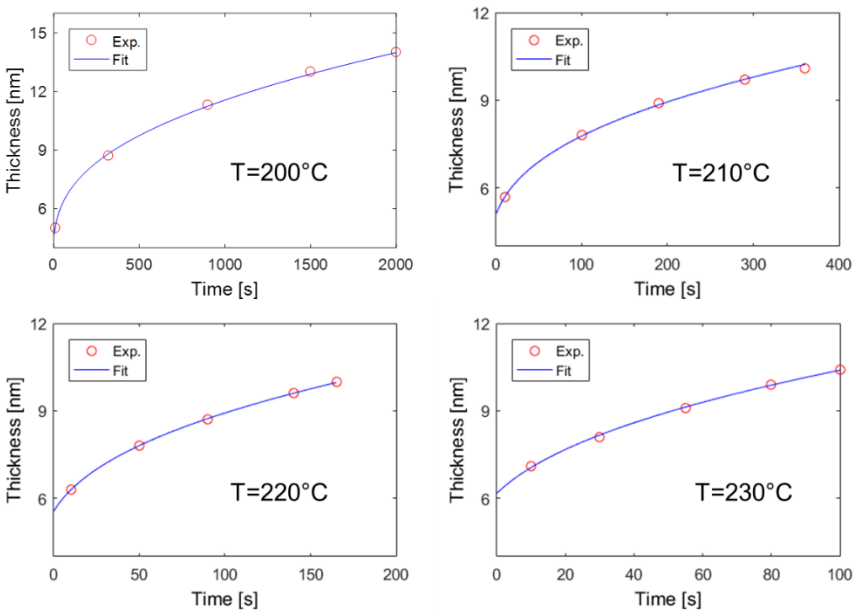

Fig. 3 : Simulation with the nonlinear reactive diffusion model (Eq. 1) of the evolution of the silicide thickness as a function of time for several temperatures of the RTA obtained experimentally for the reference sample without PAI.

Usefulness of low voltage ion milling in the preparation of TEM lamellae in microelectronic industry

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Transmission electron microscopy is widely used in the microelectronics field to achieve precise physical and chemical characterization, and to identify the root cause of electrical failures [1,2]. Regarding TEM experiment, the object under study requires to be thinned enough so as to be transparent to the electron waves. In microelectronics fields, TEM samples are usually thinned via Focus Ion Beam technique (FIB). This way, 100 nm thick TEM lamellae can be prepared. Nevertheless, some artefacts mainly ruled by ions implantation can modify the structural order by inducing some phase transition from a crystalline compound to an amorphous one. Due to the energy of FIB instrument, depending on the tension applied, ions bombardments usually promote collision cascade, mixing and recoils implantation [3]. This leads to the creation of lacuna, interstitials, and disorder at higher doses. While amorphization usually occurs on lamellae surfaces, this can induce imaging artefacts such as some blurred interfaces. Furthermore, ions implantation induced by FIB can generate locally an increase of the temperature distribution [4]. In the case of materials crystallizing in metastable phases, FIB effect could provoke phase transition. Consequently, damages promoted by FIB process can alter the material and thus limit the characterization or even induce inaccurate results. To overcome this problem, the use of low energy voltage could hence reduce damage. New FIB system gives the possibility to clean TEM lamellae using low voltages down to 500 eV. However, for certain sensitive materials such as indium or tellurium, sample preparation requires a specific study to overcome any damages. Another way would consist of using light element ions at low voltage [5]. In this study, we demonstrate that the use of argon ion as ion milling accelerated at low voltage, typically 300 eV, significantly reduces amorphization induced by FIB. TEM micrograph of backend region, illustrated in figure 1a, shows some sharp interfaces between SiO/SiN layers for a TEM lamella. This blurred effect is actually related to surface amorphization during FIB sample preparation. However, the use of argon ion milling post FIB, as seen in figure 1b, enhances the image quality and allows to distinguish clearer interfaces. This improvement is related to the cleaning of amorphous layers owing to argon ion milling. Finally, this Ar cleaning enables accurate measurements of this specimen (Fig 1b). Other experiments indicate that the use of argon milling at low voltage improves the thinning at the interface of W contact with TiN barrier. Indeed, as seen in figure 2, EELS analysis of TiN barrier does not identify any nitrogen content post FIB preparation. Certainly, this is mainly ruled by relief transfer artefacts. However, as illustrated in figure 2b, using low voltage argon enables to thin this area. First of all, the STEM image appears cleaner, and the TiN layer is clearly identified. Moreover, this thinning allows to point out a nitrogen content, as displayed on Fig2 b at nitrogen edge. Others experiments (not shown here), revealed that argon ion milling post FIB enables to prevent any structural damages by conserving metastable phase of TiSi. Furthermore, GeSbTe sample preparation using FIB and cleaned by argon ion milling evidenced a clear conservation of the structural order.

Therefore, we reported here the improvement of TEM lamellae cleaned by argon ion milling, leading to the improvement of characterization of thin interfaces and the significant utility to thin any sensitive material by preventing from any amorphization and thus conserving the local structural order.

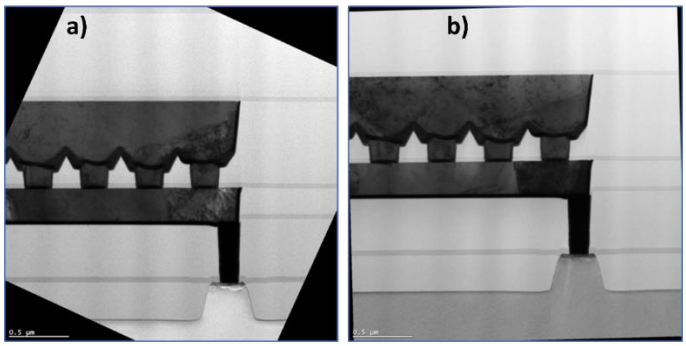

Figure 1a) Backend TEM micrograph prepared by 16 keV FIB, B) TEM micrograph of the sample cleaned by Ar ion milling

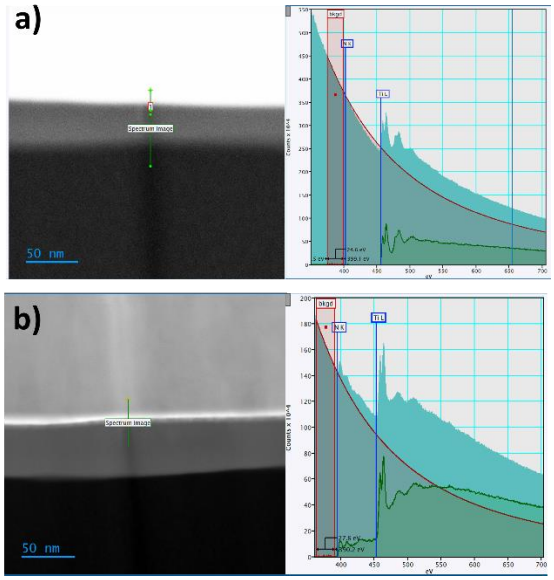

Figure 2 1a) STEM mircograph prepared by 16 keV FIB and its associated EELS spectra at nitrogen k and Ti L2,3 edges B) STEM micrograph of the sample cleaning by Ar ion milling and its EELS spectra of TiN interfaces

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From sapphire to engineered Si substrates for Ga_2O_3 heteroepitaxy: theory indications to avoid large lattice misfits

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Ga_2O_3 is a promising material for power electronic devices because of the high breakdown voltage, the huge Baliga figure of merit, and the limited thermal budget in deposition: some 500-800 °C, depending on crystal phase and epitaxial method [1]. This latter feature allows for potential integration in the Si technology, but most of the experimental and theoretical studies are focussed in deposition on α-Al_2O_3 (0001) substrates. It is clear that deposition on Si would also be suitable for heat dissipation reasons, as both Ga_2O_3 and Al_2O_3 are poor heat conductors, but some critical issues in Ga_2O_3 heteroepitaxy are present.
The first one is the large polymorphism of Ga_2O_3: β (the monoclinic and stable phase), α (the rhombohedral phase), κ (the orthorhombic phase), δ (the cubic bixbyite phase) and γ (the cubic, defective-spinel phase). The first three polymorphs are the most common ones appearing in heteroepitaxy on sapphire and are really very close in formation energy. [1,2]
The second one is the misfit in symmetry and in lattice parameters, not only with the Si faces, but also with the sapphire substrates, so that rotational domains are quite common in β and κ heteroepitaxy.
The third one is the competing Si oxidation that starts as soon as the oxygen, or water vapor, inlet sets in: either a controlled pre-oxidation is operated (such as the one with ALD or MBE equipment), or an inert buffer layer is deposited (such as 3C-SiC, compatible with Si in deposition temperature).

By a recent first-principles investigation of ours on the volume and surface energies of Ga_2O_3, with and without misfit strain on sapphire (0001) [2], we have shown that the misfit strain alters the hierarchy in energy for differ film phases and orientations, in qualitative agreement to experiments [3]. Calculations of interface energies are in progress, in order to set a quantitative ground for a nucleation and growth modelling of Ga_2O_3 islands [3], but this theoretical background is also used in order to approach the growth of Ga2O3 on SiO_x/Si substrates (thanks to an accurate modelling of the very first stages of Si oxidation, personally communicated by Alfredo Pasquarello and Angelo Bongiorno [4]), and the growth of Ga_2O_3 on 3C-SiC/Si.
We will report about the interfacial matching for different film/substrate orientations, both in terms of lattice misfit and chemical bonding, aiming at providing a systematic roadmap for improving the existing (few) experimental trials, both on Si, or SiO_x/Si, and on 3C-SiC/Si.

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Forward conduction mechanism at W-based Schottky contacts on AlGaN/GaN heterostructures

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Gallium Nitride (GaN) is considered to be a suitable material for the next generation of high power electronic devices considering the high bandgap (3.4 eV) and high critical breakdown electric field (3.3 MV/cm) [1]. Furthermore, the fabrication of AlGaN/GaN epitaxial heterostructures, due to the compresence of spontaneous and piezoelectric polarization [2], leads to the formation of a quantum confined two-dimensional electron gas (2DEG) characterized by a high electron mobility of about 2000 $cm^2V^{-1}s^{-1}$ [3]. For these reasons, high electron mobility transistors (HEMTs) based on heterostructures are captivating devices for the next generation of high-frequency applications.

The Schottky contact plays a significant role in HEMTs, modulating the amount of charge of the 2DEG channel, i.e. the channel current. The conduction mechanism at Schottky metal/semiconductor interfaces is an extremely important topic for AlGaN/GaN HEMTs. Typically, this current is rationalized by the Thermionic Emission (TE) model, and it depends on the bias applied to the contact and the energetic value of the barrier at the interface, defined as Schottky Barrier Height (SBH). In particular, the SBH represent a fundamental parameter in HEMTs technology, since it has practical repercussions on devices' performances (turn-on voltage [4], threshold voltage [5], subthreshold swing [6], and overall reliability [7]). However, the presence of the 2DEG at the AlGaN/GaN interface, as well as active participation of defects inside the semiconductor, can lead to the co-presence of other mechanisms that have to be taken in consideration for a correct interpretation of the leakage current [8-10].

In this work, we have studied the current mechanisms at the interface of a W-based Schottky metal on AlGaN/GaN heterostructures by measuring the electrical properties (I-V) of Schottky Barrier Diodes at different temperatures. In Fig. 1 is reported the semilog plot of the forward current density-voltage (J-V) characteristics of the Schottky diodes measured at temperatures that range from 25°C to 150°C. The electrical behavior of the measured J-V curves displays the presence of a knee (around 1 V at room temperature) that becomes less evident by increasing the measurement temperature. The TE model itself is not able to completely explain the behavior of the acquired J-V curves. Indeed, the first linear region of the curve (0.2 – 0.5 V) has been fitted employing the tunneling model. From the slope of these curves, it is possible to extrapolate the value of E_0 [8] defined as a tunneling parameter. Then, from the thermal dependence of E_0 it was possible to estimate a value of E_{00} = 75 meV, which represents the characteristic tunneling energy, as reported in Fig. 2.

In the second linear region (0.7 – 1.2 V) the TE model has been adopted to describe the behavior of the J-V curves. Here, from the fit of the experimental curves it was possible to extrapolate the SBH and the ideality factor. These values are extracted for each curve at different temperature (Fig. 3), and by increasing the temperature from 25°C to 150°C, there's a decrease of the ideality factor from 2.59 to 1.97, and an increase of SBH, from 0.77 to 0.93 eV.

The thermal dependence of the SBH and the ideality factor is symptomatic of an inhomogeneous contact, in fact from the analysis of the experimental data the diode is made of different regions each that contribute to the total current with a particular conduction mechanism. Indeed, considering both Tunneling and TE model, it was possible to fit the entire experimental curves. In Fig. 4 the J-V curves acquired at 25°C and 150°C has been displayed as an example. In particular, it can be seen that at low bias (<1 V) the tunneling mechanism has the highest contribution to the total current density, while at high bias (>1 V) the TE mechanism prevails.

Increasing the temperature makes the TE model to be the most predominant mechanism over a wider range of applied bias even at bias lower than 1 V.

These results highlight the inhomogeneity nature of the Schottky contact on AlGaN/GaN heterostructures, and the prevalence of the Tunneling or TE model indicated by the evident knee in the experimental J-V curves depending on the temperature and the applied bias.

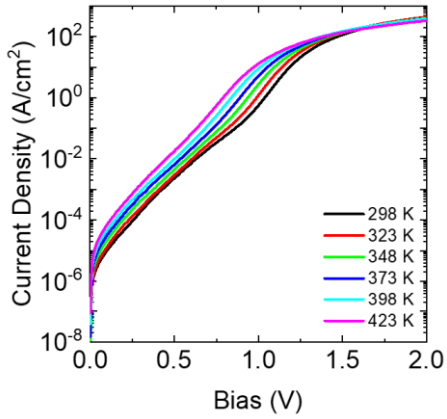

Fig 1. Experimental J-V curves measured at different temperatures.

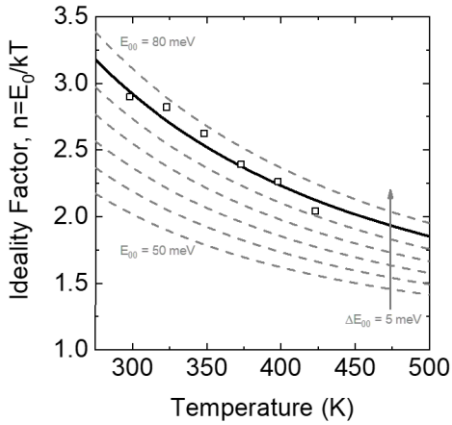

Fig 2. Temperature dependence of the ideality factor and simulation of ideality factors for arbitrary E_{00} values.

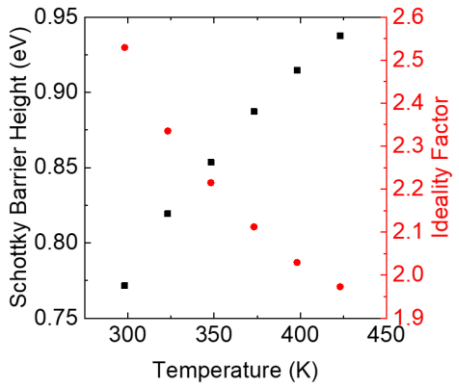

Fig 3. Temperature dependence of the ideality factor and the Schottky Barrier Height from TE mode.

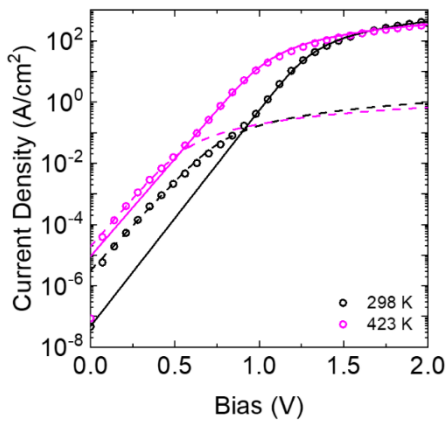

Fig 4. Experimental and fitted J-V curves according to the Tunneling model (dashed lines) and the TE model (solid lines) at 25°C and 150°C.

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Influence of annealing schemes on the formation and stability of Ni(Pt)Si thin films: partial, laser, total, and unique anneals

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Silicide thin films are used as contacts to improve electrical conductivity in microelectronics technologies [1]. For advanced technologies (starting from the 65 nm-node), the choice of silicide material has converged towards nickel-based silicide: Ni(Pt)Si thin films. Compared to the previously popular cobalt-based silicides, Ni(Pt)Si presents the advantage of a lower formation temperature, and a diffusion-controlled growth, preventing formation issues in narrow active lines [1]. However, one of the major drawbacks of Ni(Pt)Si films is their low stability at high temperatures *i.e.,* morphological degradation due to the agglomeration phenomenon. With the downscaling trend of the transistors, the current thickness of Ni(Pt)Si films is reduced to 10 nm resulting in a high sensitivity to agglomerate. Such degradations represent a serious limitation particularly in recent imagers technologies dealing with the co-integration of both Ni(Pt)Si and $TiSi_x$-based contacts [2]. In addition, due to the reduction of final Ni(Pt)Si thickness obtained through laser anneal, Dynamic Surface Annealing (DSA) has been introduced for the 28 nm-FDSOI technologies instead of the classical Rapid Thermal Annealing [3].

In a previous work, we demonstrated that the annealing schemes (partial, total, and unique anneal) used during the formation of Ni(Pt)Si thin film impact the final silicide thickness, microstructures and agglomeration temperature [4]. Previous findings indicated that a potential impact of the silicide film texture might explain the results discrepancy.

In this study, the impact of various annealing schemes (partial, DSA, total, and unique anneal) on the formation and agglomeration of ultra-thin Ni(Pt)Si films is investigated. In this way, similar Ni(Pt)Si thickness (10 nm) has been achieved on 300 mm Si(100) wafers. After complete formation, the silicide films are then submitted to an additional anneal, between 500 and 800 °C, to evaluate their stability at high temperatures (Fig. 1). To this extent, a combinatorial approach of several ex-situ techniques (Rs, ellipsometry, TEM-EDX, SEM, and EBSD) is performed.

Fig. 2 illustrates that the degradation of Rs appears to shift to higher or lower temperatures depending on the annealing type. One might consider that this result could not be assigned to a discrepancy in final silicide thickness. Moreover, on Fig. 3, top-view SEM inspections performed after the additional annealing at 500 °C for 30 s demonstrates a change in silicide microstructures, and confirms the previous Rs results indicating that DSA anneal allows to delay the degradation to high temperatures (Figs. 2 and 3). Our findings suggest that the pink-NiSi(013) grains, in Fig. 4, present a more favourable interface energy with the Si(100) substrate as compared to the blue-NiSi(100). The pole figures presented in Fig. 5 explicit an axiotaxy-like texture in the particular case of DSA annealing. Texture comparisons for ultra-thin films (10 nm) give deeper insights into the role of the orientations of NiSi(010) and NiSi(013) in the agglomeration phenomenon. Depending on the annealing schemes used during the formation of the silicide, there is a strong correlation between the initial microstructures of Ni(Pt)Si films and the agglomeration. Indeed, cross-analyses of these different key parameters indicates that the presence of very fine grains (40 nm) in DSA-laser anneal, and high ratio of Ni(Pt)Si grains oriented towards the (013) direction (or pink-indexed grains) appear to be more efficient in delaying the agglomeration to higher temperatures. These results will be discussed in terms of grain size distribution by combination of SEM and TEM analyses, elements redistributions by STEM-EDX profile scans, and texture evolutions during agglomeration by pole figure and EBSD analyses.

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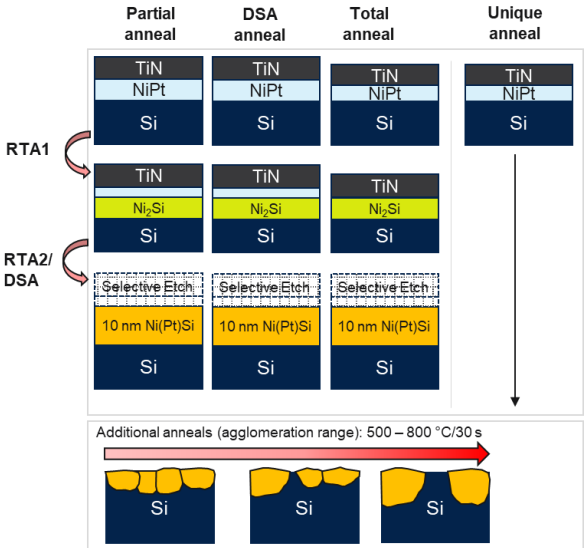

Fig. 1: Schematics of the different annealing schemes used during the formation process of 10 nm Ni(Pt)Si films followed by an additional high temperature-anneals between 500 – 800 °C/30 s.

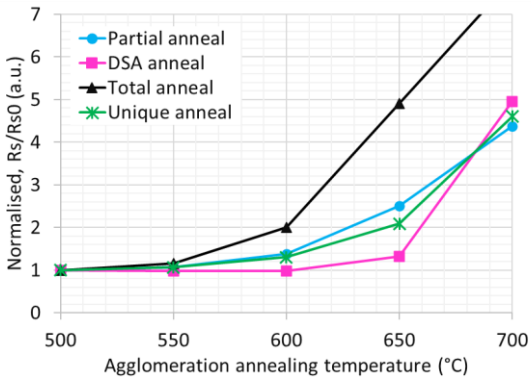

Fig. 2: Normalized sheet resistance, Rs, of 10 nm Ni(Pt)Si formed by different annealing schemes post-high temperature anneals showing drastic Rs increase due to film degradation.

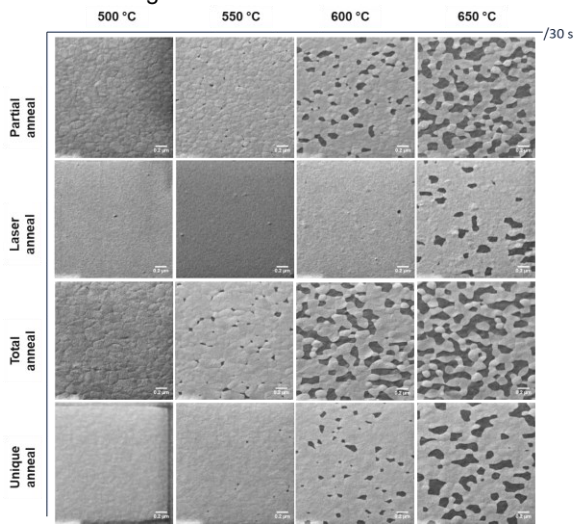

Fig. 3: Top-view tilted-SEM images of 10 nm Ni(Pt)Si illustrating morphology evolution during agglomeration phenomenon for annealing between 500-650 °C/30 s. Light gray contrast represents Ni(Pt)Si thin film, dark gray contrast represents exposed Si substrate.

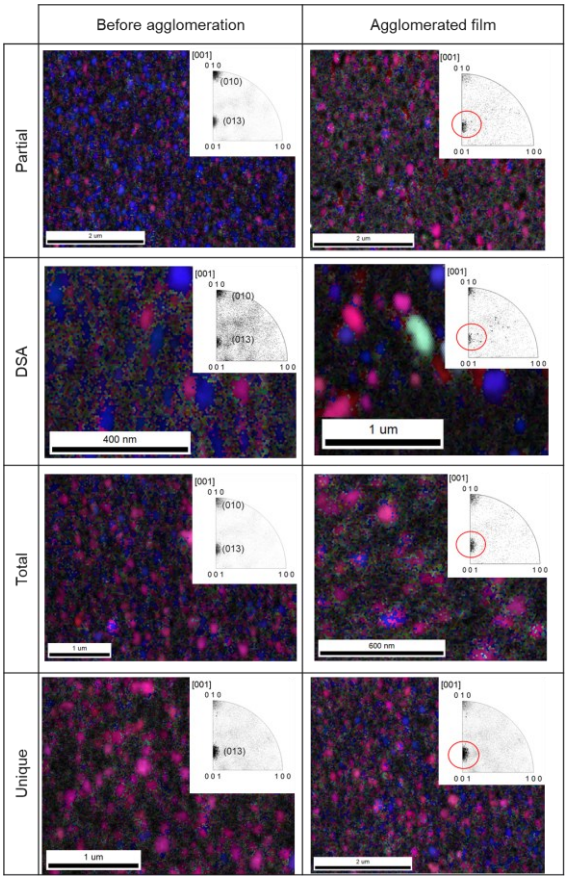

Fig. 4: EBSD cartography mappings and inverse pole figures (IPF) for grains spatial distribution and texture analysis of Ni(Pt)Si on Si(100) substrate. Pink colour represents Ni(Pt)Si(013)/Si direction, blue represent Ni(Pt)Si(010)/Si(100) direction and dark areas represents unindexable and/or fine grains. Texture evolves principally towards pink grains after agglomeration as seen in IPF where intensity of Ni(Pt)Si(010) is reduced while Ni(Pt)Si(013) remained.

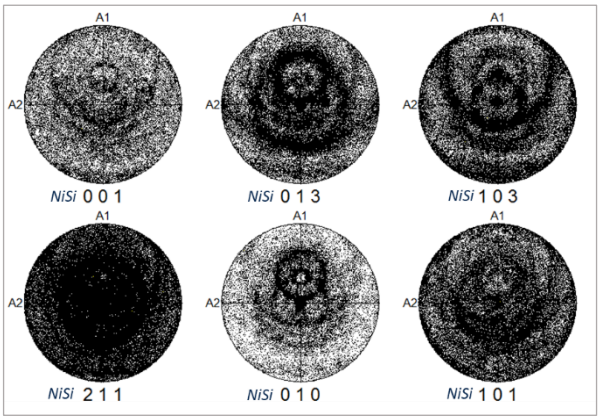

Fig. 5: EBSD extracted pole figures (PF) of 10 nm Ni(Pt)Si film on Si(100) substrate formed by DSA after annealing at 550 °C/30 s. Axiotaxy-like texture is detected in the typical axiotaxy direction *i.e.,* NiSi(013), NiSi(211), and NiSi(202).

Electrochemical Deposition of Nanotwinned Cu in Damascene Features

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We have explored electrochemical deposition of highly (111) oriented nanotwinned (nt-)Cu [References 1-4] in damascene features. Electrochemical deposition of nt-Cu was tested initially on a coupon-scale and after process optimization transferred to (∅300mm) wafer-level commercial plating tool. The goal was to deposit nt-Cu without having to modify hardware on the plating tool, resorting to complex deposition waveforms or other experimental parameters/setups atypical for Cu plating of ∅300mm wafers.

Successful deposition of nt-Cu on ∅300mm blanket wafers and tuning of the Chemical mechanical polishing (CMP) processing was followed by first tests on patterned damascene structures. Quality of the Cu fill was checked against different feature sizes and their aspect ratios (AR). Cylindrical (disc) damascene structures had diameter ranging from 1 to 100 micron and depth from 500 nanometers to 2 microns. Figure 1 shows cross section FIB image zoomed-in on the central part (not showing field and sidewalls) of the 2-micron deep feature having diameter of 20 microns. Please note that no characteristic pyramids on top of highly (111) oriented nt-Cu are observed since Cu overburden has been CMP-ed prior to FIB analysis.

We report on the feature size and AR dependence of the Cu fill, degree of (111) orientation of plated Cu, thickness of the transition zone and other properties relevant for electrochemically deposited nt-Cu. Based on the collected data, we attempt to extrapolate the findings to feature sizes and AR that could be relevant for future applications.

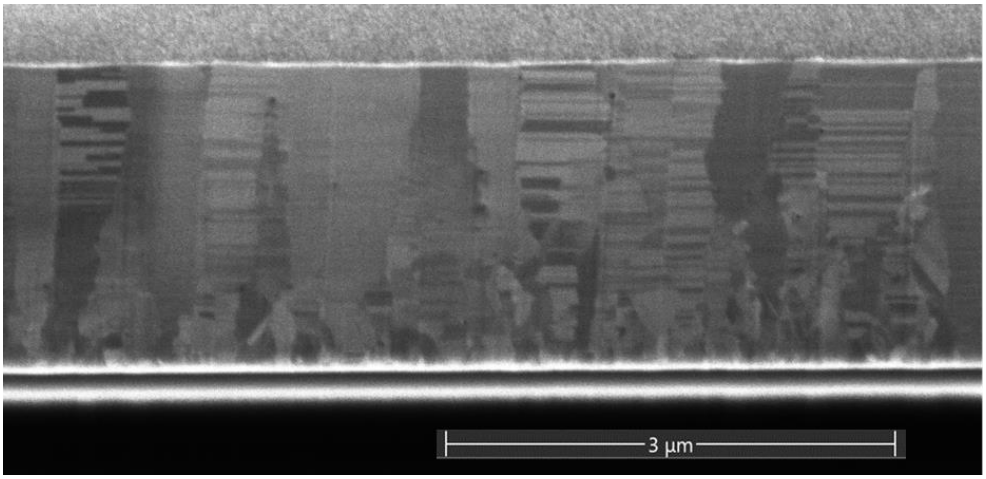

Figure 1. Cross-section FIB image of the central part of the nt-Cu filled damascene feature. CMP has been performed prior to FIB analysis and Cu overburden removed.

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Thermally Stable Ohmic Contacts on GeSn Layers

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Germanium tin doped (GeSn) alloy, unlike germanium, is a direct bandgap semiconductor, making it a good candidate for optoelectronic applications [1]. The most commonly used process for making an ohmic contact on germanium is nickel deposition and diffusion, which occurs during rapid thermal annealing to produce a stable Ni-Ge alloy with low sheet resistance and low specific contact resistance. However, if the tin addition does not change this phase sequence, Sn segregates at temperatures higher than 350 °C and affects the sheet resistance of the alloy [2]. Such phenomena limit the integration of GeSn alloys on a Si CMOS platform where the thermal budget during fabrication is important. An alternative presented in this work is the use of titanium metallization on GeSn alloy [3].

N-type GeSn layers with 6 at.% of Sn ([P] = 3E19 at/cm^{-3}) were epitaxially grown on Ge-buffered Si (100) substrates in a reduced pressure chemical vapor deposition (RP-CVD) tool. A surface preparation was performed by Ar plasma treatment for 60 s. Then, Ni, Ti and TiN capping films were deposited by magnetron sputtering at room temperature. Various physicochemical characterizations were performed, including AFM, XRD and sheet resistance (R_{sh}) measurements. Transfer length measurement (TLM) structures were fabricated to extract the contact resistivity.

Titanium reacts with GeSn to form a stable Ti-rich alloy (at least up to a certain temperature threshold), which has a low sheet resistance like NiGe(Sn). The study of the annealing of titanium on GeSn (Fig. 1) shows that the surface morphology remains little deteriorated up to 450 °C compared to the Ni / GeSn system.

Square TLM tests were performed for both Ni and Ti contacts. The results of the Ni contact (Fig. 2) show a rather low contact resistivity with a value around 1.4 x 10^{-5} Ohm.cm^{-2} after a 250°C annealing. Above 350 °C, the Ni-based contacts are no longer ohmic. This is probably due to NiGe agglomeration and Sn segregation phenomena [4]. The Ti metallization (Fig. 3) shows interesting behaviour. Thin Ti film has relatively low contact resistivity as deposited (about 1.5 x 10^{-5} Ohm.cm^{-2}), but contact deteriorates sharply at temperatures above 250 °C. 10 nm Ti deposition shows the lowest contact resistivity with a stable trend up to 350 °C. The best value obtained is 8 x 10^{-6} Ohm.cm^{-2} as-deposited. The thick 20 nm Ti layer gives a higher contact resistivity as deposited, but the values decrease with increasing annealing temperature to reach about 1.75 x 10^{-5} Ohm.cm^{-2} at 400 °C.

This study shows that Ti-based contacts are a viable alternative to obtain thermally stable contact on GeSn layers. Other technological levers to achieve stable Ni / GeSn contacts will be discussed.

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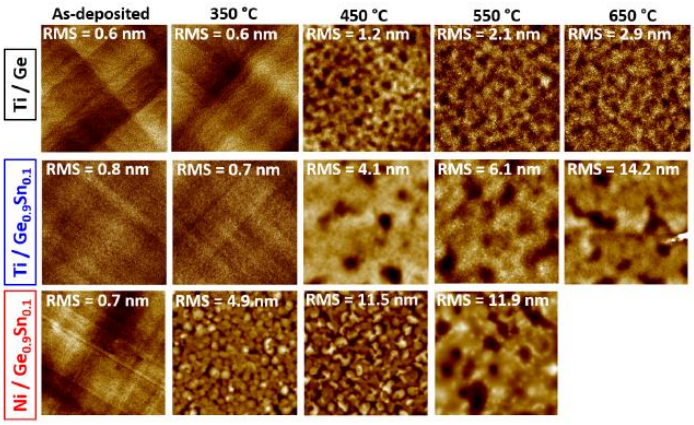

Figure 1: Surface AFM images (scan size 5 µm × 5 µm) of metal / Ge or GeSn samples annealed at various temperatures under N_2 [5].

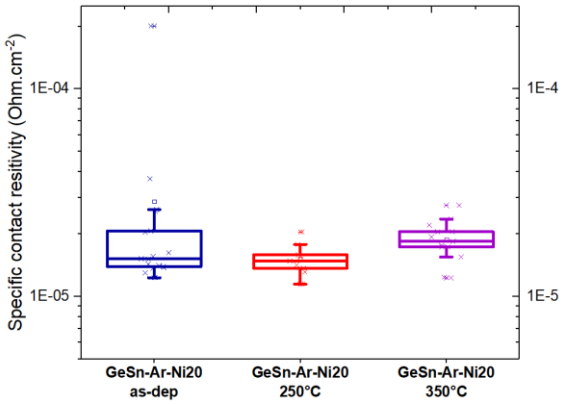

Figure 2: Contact resistivity values obtained from TLM for as-deposited or annealed Ni metallization.

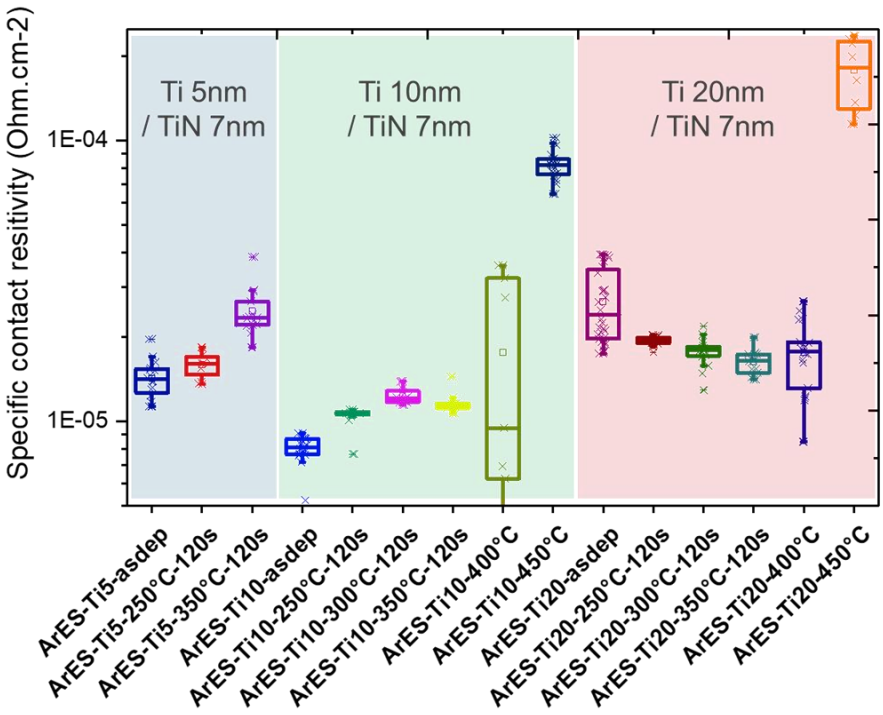

Figure 3: Contact resistivity values obtained from TLM for as-deposited or annealed Ti metallization..

Parylene C as a memristive material for biocompatible memory and synaptic devices

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Even though established von Neumann architectures are extremely powerful and state of the art for the current computer generation, they are not suitable for upscaling and the realization of the next computer generation. To enable future technologies such as artificial intelligence, particularly they lack of parallel data processing as well as they feature low integration densities and a high-power consumption. Hence, new approaches of computing architectures are required for the future. Doing so, neuromorphic computing based on memristive devices seems promising in order to avoid the shortages given above. Furthermore, they are suitable for the data processing on site, i.e. edge computing, as well as the data processing based on memory devices, i.e. in-memory-computing. Considering these features in combination with their low energy consumption, neuromorphic architectures can be used for wearables as well as medical implants. However, for these applications the usage of only biocompatible materials is essential. Additionally with respect to wearables, flexibility of the material is crucial.

Parylene is a family of thermoplastic polymers with a unique combination of excellent properties. These include biostability and biocompatibility according to ISO 10993, dieletric properties, low permeabilities for gases and water vapor, mechanical stability and bendability even at low thicknesses, optical transparency as well as chemical inertness against all common acids, bases and solvents. Particularly the latter enables the compatibility of parylene with established micromachining technologies. Parylene is deposited by chemical vapor deposition (CVD) according to the Gorham process, which includes the polymerization at room temperature. Hence, the deposited are free of any intrinsic stresses. Considering the given properties, parylene can be used as a barrier layer for encapsulation, as a dielectric layer for electrical insulation as well as an ultra-thin freestanding substrate for flexible electronics. [1;2]
Besides these three functionalities, the aim of the presented research was to investigate, whether parylene can be used as a memristive material to establish a fourth functionality. Doing so, memristive test architectures, i.e. metal-insulator-metal (MIM) stacks, were fabricated on 200 mm silicon wafers (Fig. 1). In a first step, silicon dioxide was thermally grown for isolation, followed by subsequent sputtering of titanium nitride as a diffusion barrier. Next, platinum electrodes with a titanium adhesion promoter were sputtered. The parylene C was deposited by chemical vapor deposition with thicknesses of 60 nm, 125 nm, 250 nm and 500 nm, respectively. Finally, the top electrode was realized by sputtering copper for electrochemical metallization (ECM), followed by platinum and aluminum for reliable probing. All three top layers were deposited using a silicon shadow mask with square openings of 100 µm², 150 µm², 250 µm², 400 µm², 600 µm², 1000 µm², 2000 µm² and 3000 µm², respectively. For characterization, the current-voltage-dependencies for all structures were measured using a wafer prober.

A typical current-voltage-dependency is depicted in Fig. 2. In summary, for parylene thicknesses of 60 nm, the growth of filaments could be easily initiated by the application of a voltage. For the different sizes given above, no area dependency was observed. Hence, it can be concluded that the mechanism is based on mono filaments. For parylene thicknesses of 125 nm, initially no growth of filaments could be stimulated. However, after three months storage at ambient temperature, memristive behavior was observed though. Thus, it can be concluded that the filaments were induced by diffusion of the copper electrode. At higher thickness of parylene, i.e. for 250 nm and 500 nm parylene thickness, only capacitive behavior was observed. In conclusion, the optimal parylene thickness is expected to be between 60 nm and 125 nm. As can be seen in Fig. 2, the hysteresis loops are comparably small, however, they are quite stable and feature a good reproducibility. Furthermore, the voltages and currents are comparably low, which makes the parylene memristor technology attractive for low-power applications. The presented research paves the way for establishing parylene as a memristive material and hence, neuromorphic computing on ultra-thin, flexible devices.

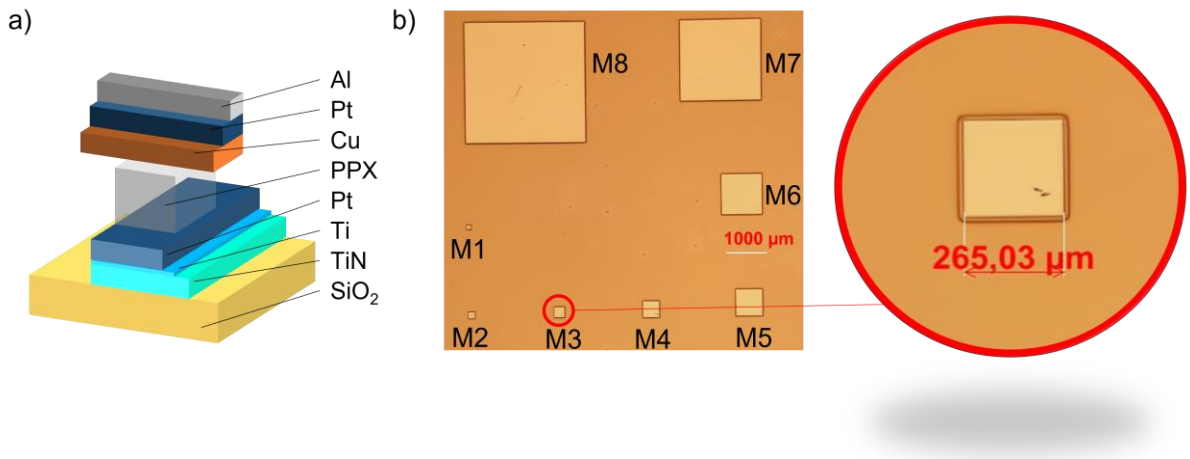

Figure 1: a) Layer structure of the memristive parylene device and b) microscopic image of a reticle with different memristor sizes (M1 - M8).

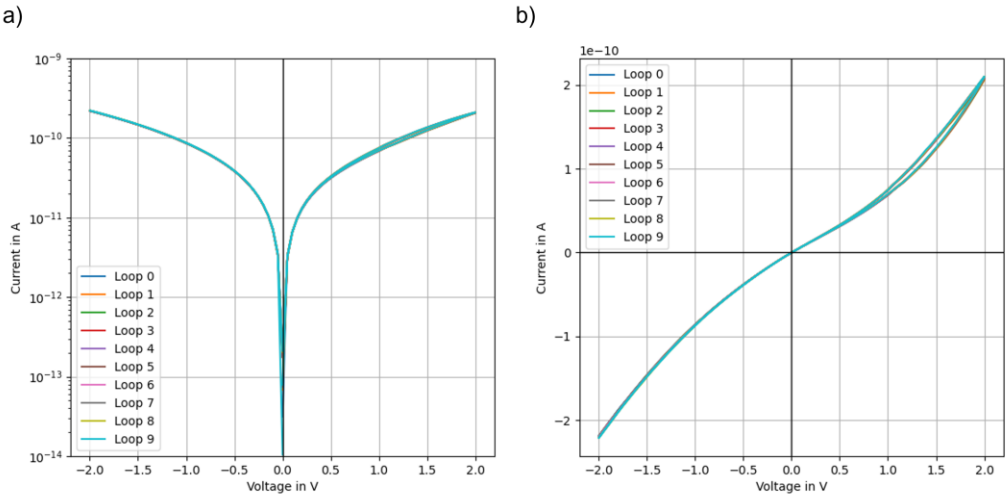

Figure 2: Ten hysteresis loops of a M3 parylene memristor with 60 nm parylene thickness and with currents in the picoampere range in a) logarithmic and b) linear scale.

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Effect of Ni on the formation of Co silicides from Co-Ni alloy.

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In microelectronics, especially in Complementary Metal Oxide Semiconductor (CMOS) technology, metal silicides such as Titanium disilicide ($TiSi_2$), Nickel monosilicide (NiSi), and Cobalt disilicide ($CoSi_2$) have been widely used as contacts (i.e., to form source, drain and gate contacts) [1]. Although NiSi is mainly used for sub-65 nm CMOS technology, it is interesting to use the low resistivity of $CoSi_2$ for 65 nm CMOS technology, especially in 200 mm fabs [2]. However, the formation of $CoSi_2$ is difficult in small devices, especially with sizes below 65 nm and lower formation temperatures are required for the actual process. Several studies have demonstrated that adding/alloying Ni (i.e., ternary $Co_{1-x}Ni_xSi_2$) significantly reduces the formation temperature of the $CoSi_2$ phase [3,4]. Moreover, the alloyed films are morphologically more stable and offer a smaller lattice mismatch to Si than non-alloyed films ($NiSi_2$ and $CoSi_2$). Hence, understanding the impact of Ni incorporation on the formation of $CoSi_2$ is needed.

Therefore, in this work, we systematically investigated the effect of different Ni concentrations (i.e., 0 at.%, 8 at.%, 15 at.% and 35 at.%) on the formation of Co disilicides. After cleaning the substrate (i.e., Si_{100}), Co(Ni) films were deposited using simultaneous magnetron co-sputtering of Co and Ni targets. During this co-deposition, the substrate was not rotated in order to obtain a gradient of Ni concentration in the Co film. The powers applied on the Co (P = 150 W) and Ni (P = 30 W) targets during the co-sputtering were optimized in order to obtain Ni concentration varying between 2 and 45% and thicknesses between 30 and 90 nm by comparing simulation (Fig. 1a) and experimental measurements of the thickness by XRR (Fig. 1b) and Ni content by SEM/EDX. Later, a 30 nm SiO_x protective layer was deposited in order to carry out the in-situ XRD measurement (Fig. 2), and the results show that the same formation sequence (i.e., Co_2Si, CoSi and $CoSi_2$) is obtained for all different Ni concentrations. Noticeably, the texture of the films varied with respect to the Ni concentrations, mainly the preferential orientation of the $CoSi_2$ phase (i.e., 220, $2\theta = 47.8°$) intensity is highly enhanced with 8 at.% and 15 at.% of Ni films than the pure one (0 at.%). However, the presence of the NiSi phase (i.e., $2\theta = 31.6°$ & 35.7°) is noticed for a higher Ni concentration (i.e., 35%, see Fig. 2d) than other concentrations. This NiSi phase formation (below 350 °C) for the initial concentration of 35% Ni is related to the solubility limit of Ni in CoSi (about 30 at.% of Ni at 400 °C). Indeed if the concentration is higher than the solubility (i.e., 35 at.% Ni instead of 30 at.%), it does not allow the incorporation of all Ni within the CoSi phase, leading to formation of the NiSi phase (Fig. 3). Furthermore, the evaluation of the $CoSi_2$ phase formation temperature is spotted with various Ni concentrations (Fig. 4), for example, 515 °C (0 at.% Ni), 470 °C (8 at.% Ni), 445 °C (15 at.% Ni), 490 °C (35 at.% Ni). As a result, adding a small Ni concentration that favors the $CoSi_2$ phase formation at a lower temperature, even for the larger Ni quantity (35 at.%), is still below the temperature range than pure Co one (i.e., 0 at.% Ni). These results may be explained using the ternary phase diagram (Fig. 3). Hence, this study is beneficial to understanding the impact of Ni on the Co silicide formation and to the integration of Co(Ni) alloys for contact formation in microelectronics.

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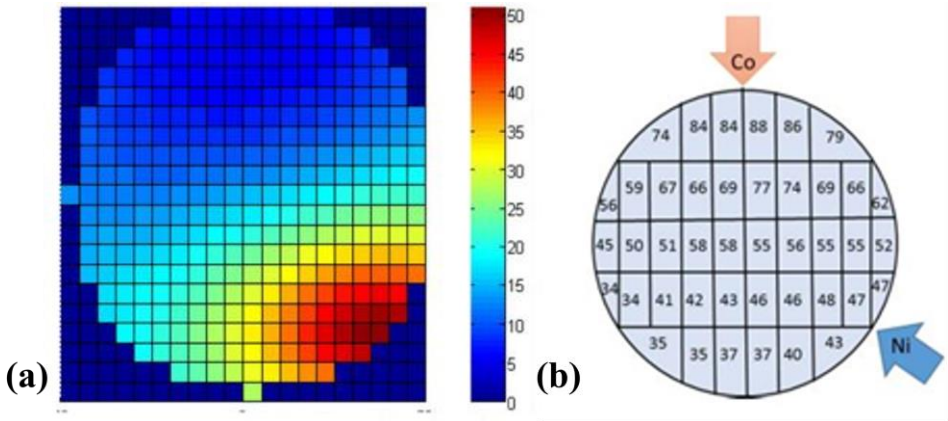

Fig. 1: Co-deposition of Co & Ni: (a) Simulated gradient of Ni percentage and (b) Thicknesses measured by XXR.

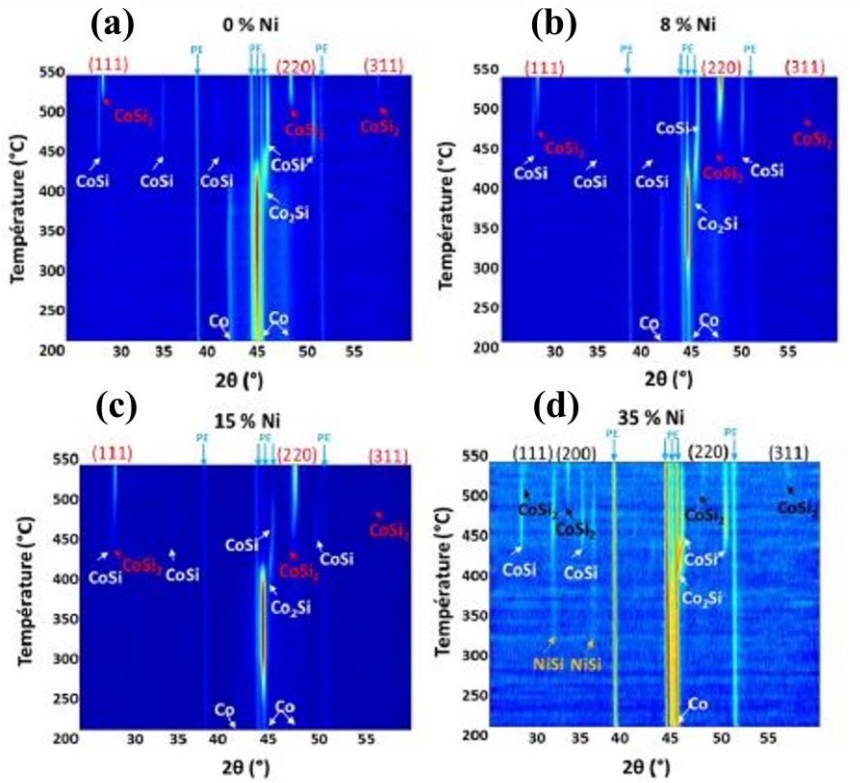

Fig. 2: In-situ XRD patterns for different Ni concentrations (a) 0 at.%, (b) 8 at.%, (c) 15 at.%, and (d) 35 at.%.

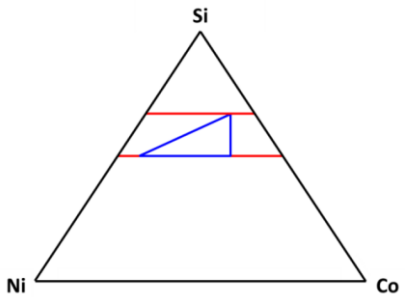

Fig. 3: Co-Ni-Si ternary diagram at 450 °C showing the equilibrium between CoSi, NiSi and $CoSi_2$.

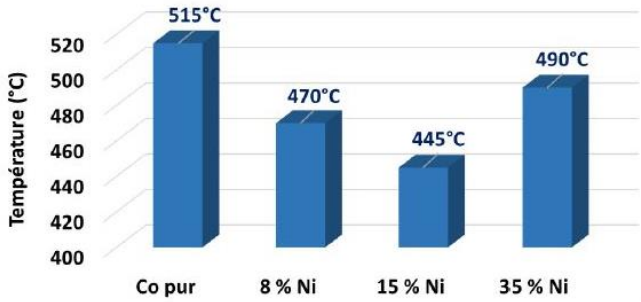

Fig. 4: Formation temperature of $CoSi_2$ phase using different Ni concentrations (0 at.%, 8 at.%, 15 at.%, and 35 at.%).

Investigation of carbon-cap formation by thermal CVD using ethanol for ruthenium and molybdenum

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Graphene-capped copper (Cu) interconnects are attracting attention as a candidate for the next generation of low-resistance nano-interconnects.[1] It has also been reported that covering the surface of ruthenium (Ru) with graphene reduces resistance. [2] Molybdenum (Mo), like Ru, is a candidate as an MOL metal, but suppression of surface oxidation is an issue. [3] We previously reported that surface oxidation can be suppressed by depositing a carbon (C) cap on a nickel surface by thermal CVD at a low temperature of 350°C. [4] The objective of this study is to examine whether the thermal CVD could be applied to Ru and Mo.

A 30 nm thick film of Ru and Mo was deposited by sputtering on a Si substrate (8 inch) with a 100 nm thick thermal oxide film. For Ru sputtering, tantalum (Ta) with a thickness of 3 nm was deposited prior to Ru sputtering as an adhesion layer. The substrate cut into 1 cm squares was placed inside the quartz tube of the CVD apparatus reported previously, [4] heated in an electric furnace to the set temperature between 300 and 700 ℃ in an Ar atmosphere at normal pressure, and when the set temperature was reached, ethanol bubbled with Ar was supplied for 10 minutes. The CVD conditions are the same as those previously used for Ni. [4] For comparison, samples annealed without flowing ethanol were also prepared. For evaluation, C deposition was investigated using Raman spectroscopy, and sheet resistance before and after CVD or annealing was measured using a four-point probe method. SEM, XPS, and XRD were used for analysis.

Fig. 1(a) and (b) show the Raman spectra after CVD on Ru and Mo, respectively. No carbon deposition was observed on Ru at any temperatures. On the other hand, G and D band features were observed on Mo, indicating amorphous C deposition. No obvious dependence on temperature was observed. Fig.2 (a) and (b) show the resistivity changes of Ru before and after CVD and annealing, respectively. Although the initial resistivity varied probably due to the variations in film thickness, the resistivity of Ru decreases after CVD or annealing. According to SEM observation and XRD, the reason for the decrease in resistance is considered to be grain growth. It is noted that the reduction ratio of resistivity was greater with CVD than with annealing at 500℃. The reason is thought to be that surface oxidation of Ru was suppressed in the case of CVD, as shown in Fig. 3, which shows a comparison of the composition depth profiles by XPS. In the annealing in this experiment, it is considered that surface oxidation of Ru occurred due to residual oxygen, but it is possible that either the residual oxygen was removed or the oxidized Ru was reduced by flowing ethanol gas. In contrast to Ru as shown in Fig. 4(a) and (b), no decrease in resistance was observed for Mo after CVD or annealing, but rather the resistance increased at 700°C. As a result of XRD analysis in Fig. 5, molybdenum carbide peaks were observed in the sample after CVD at 700°C, and molybdenum oxide peaks were observed in the annealed sample. From this result, it is considered that a low temperature at which carbide is not formed is desirable when depositing a carbon cap on Mo.

In this study, we investigated the possibility of C cap formation by thermal CVD using ethanol on Ru and Mo, which are candidate metals to replace Cu or W. In Ru, surface oxidation was suppressed under an argon atmosphere with ethanol flowing, and resistivity was reduced due to grain growth, but no C deposition was observed. On the other hand, with Mo, C deposition was observed even at low temperatures, but no reduction in resistivity was observed. Further studies will be necessary to explore the possibilities of using CVD conditions, such as increasing the flow rate and plasma CVD.

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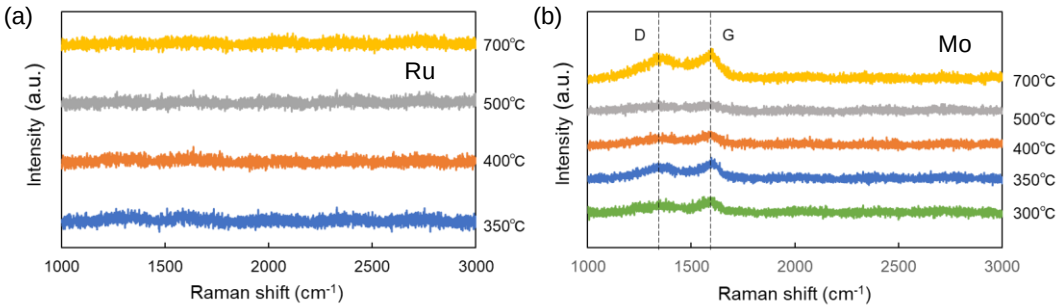

Fig. 1. Raman spectra after CVD between 300℃ and 700℃ on (a) Ru and (b) Mo.

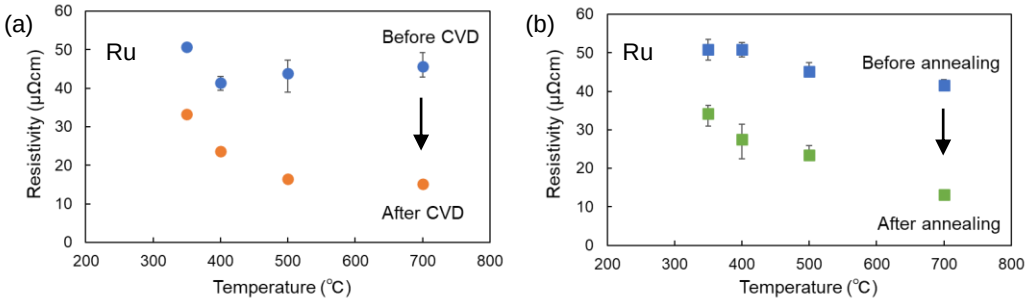

Fig. 2. Resistivity changes of Ru before and after (a) CVD and (b) annealing. Variations in resistivity before CVD or annealing may be due to variations in film thickness.

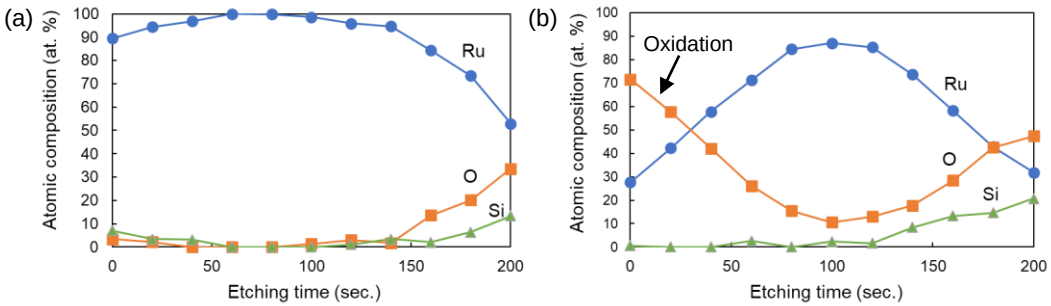

Fig. 3. Composition depth profiles of Ru films by XPS (a) after CVD and (b) after annealing at 500℃.

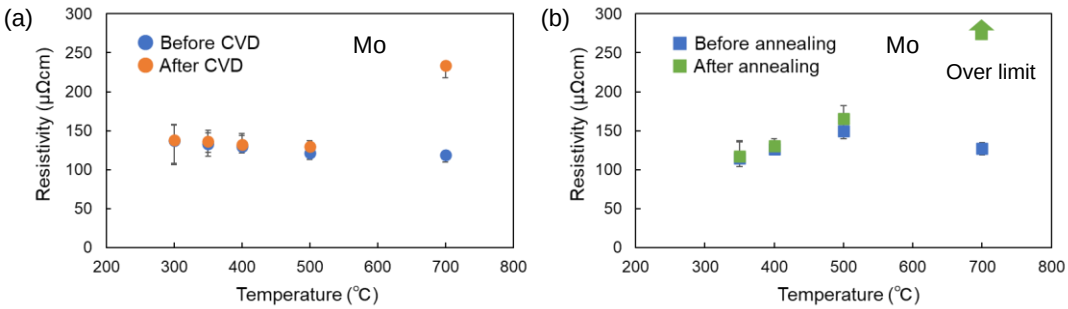

Fig. 4. Resistivity changes of Mo before and after (a) CVD and (b) annealing. Variations in resistivity before treatment may be due to variations in film thickness.

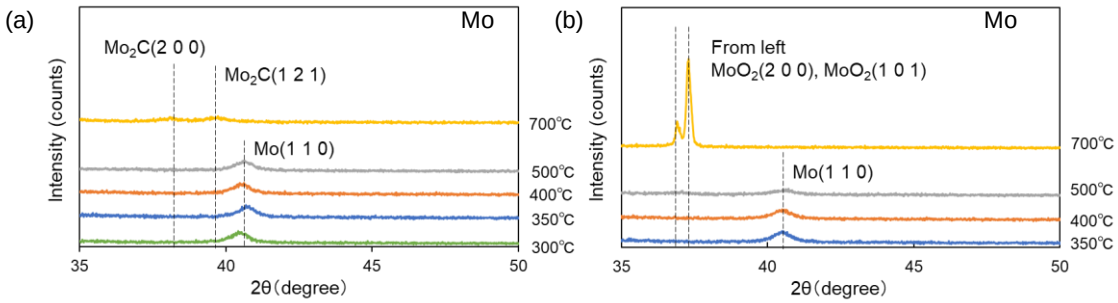

Fig. 5. XRD patterns of Mo films (a) after CVD and (b) annealing at temperatures between 300℃ and 700℃.

Strategic Superposition: Sb2Te3/TiTe2 Superlattices Possess a Low Thermal Conductivity Contrast, Ideal for PCM

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Introduction

Reducing the energy consumption of phase change memory (PCM) is one of the biggest hurdles towards its implementation. The switching mechanism in PCM consists of applying enough heat to the material to change it from crystalline to amorphous or vice versa. Diffusion of this heat into the surroundings of the cell is therefore detrimental. The thermal conductivity of the phase change material and its surroundings plays a crucial role in reducing the energy needed for a PCM to function. A good PCM material should have low thermal conductivity in both its crystalline and amorphous phase. Typical materials such as GST on the other hand, display a significant contrast in their thermal conductivity [2]. As a possible improvement we study $Sb_2Te_3/TiTe_2$ superlattices, a material system first proposed by Shen et al. in reference [1] showing a significant reduction in its reset power consumption. After deposition and structural characterization of these superlattices, the thermal transport properties are examined using time-domain thermoreflectance (TDTR).

Methods

All samples are created through magnetron co-sputtering from elementary pure targets in a variation of the modulated reactants method [3]. This method has been shown to create high-quality and planarly texturized layers with the *00L* family of planes parallel to the substrate upon crystallization. This is verified through *in situ* and *ex situ* XRD and rocking curve analysis. Time-domain thermoreflectance (TDTR) measurements are performed in a two-tint setup. This a laser pump-probe technique with which the cross-plane thermal conductivity of thin films can be accurately measured. These measurements are performed at room temperature for different thicknesses and at increased temperatures under an inert atmosphere to study the evolution of the thermal conductivity upon crystallization.

Structural Characterization

XRD patterns for films of the individual materials as well as their superlattice can be seen in figure 1. The intensity and presence of the *00L* peaks are indicative of a strong crystalline texture of the films. The evolution of an as-deposited superlattice upon anneal is visible in figure 2. Crystallization and melting of Sb_2Te_3 are visible. The intense satellite peaks are indicative of the layered structure [4].

Thermal Conductivity Results

TDTR results of single-layer samples of the individual materials are shown in figure 3. Both materials show a relatively low thermal conductivity in their as-deposited state, while (further) crystallization upon anneal increases it. The *in situ* data for a single 80nm Sb_2Te_3 layer can be seen in figure 4 where it is presented next to data for 16-period thick superlattices. A set of three types of superlattice is studied: 5nm of Sb_2Te_3 is combined with either 3nm, 6nm or 9nm $TiTe_2$. At room temperature we see that the relative composition has little effect on the as-deposited samples. This can be explained by the high thermal resistance of the amorphous Sb_2Te_3 sub-layers that dominate the stack. During anneal the thermal conductivity of all superlattices increases. Although upon cooling down, the value for the 5-3 superlattice drops down to the same value as before the anneal, reducing all contrast in thermal conductivity between the crystalline and amorphous phase.

Conclusions

The superlattice consisting of 5nm Sb_2Te_3 and 3nm $TiTe_2$ shows a minimal contrast in thermal conductivity between its two phases at room temperature, making it better suited than a single layer of Sb_2Te_3 for use as a phase change material. All superlattices demonstrate a lower thermal conductivity than the bulk as well as a decreased contrast. This might indicate that the superlattice's added interfaces not only introduce a thermal resistance, but also influence the phononic landscape, leading to the low thermal conductivity contrast that is observed.

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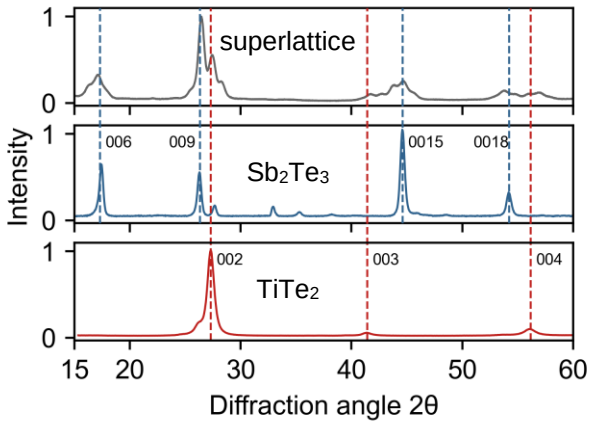

Fig. 1: The XRD pattern of an annealed superlattice shows peaks of both bulk Sb_2Te_3 and $TiTe_2$. The presence of satellite peaks is indicative of the superlattice structure.

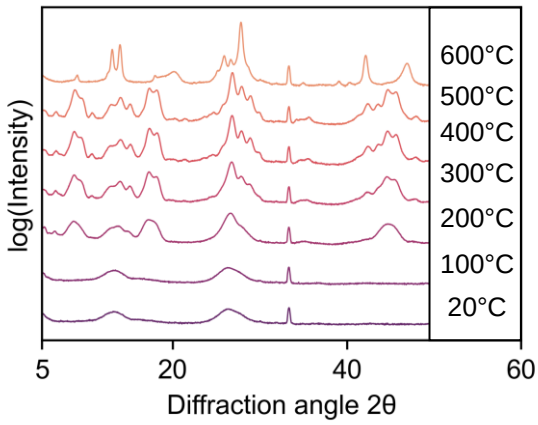

Fig. 2: *Ex situ* scans of a superlattice annealed at different temperatures show the crystallization and subsequent melting of Sb_2Te_3 .

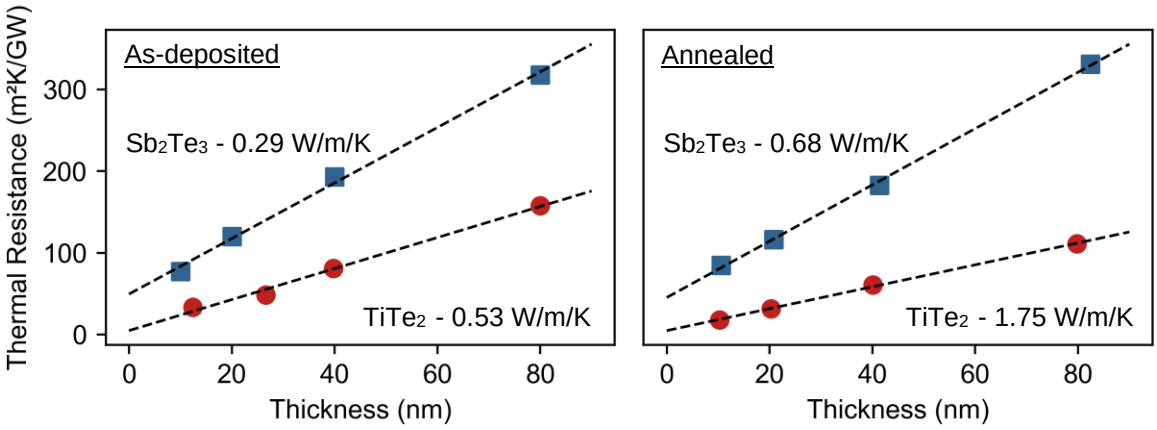

Fig. 3: The intrinsic thermal conductivity of the single layer materials is calculated by combining results for several thicknesses and performing a linear fit. These results show the thermal conductivity contrast between as-deposited samples and after a 300°C ramp anneal.

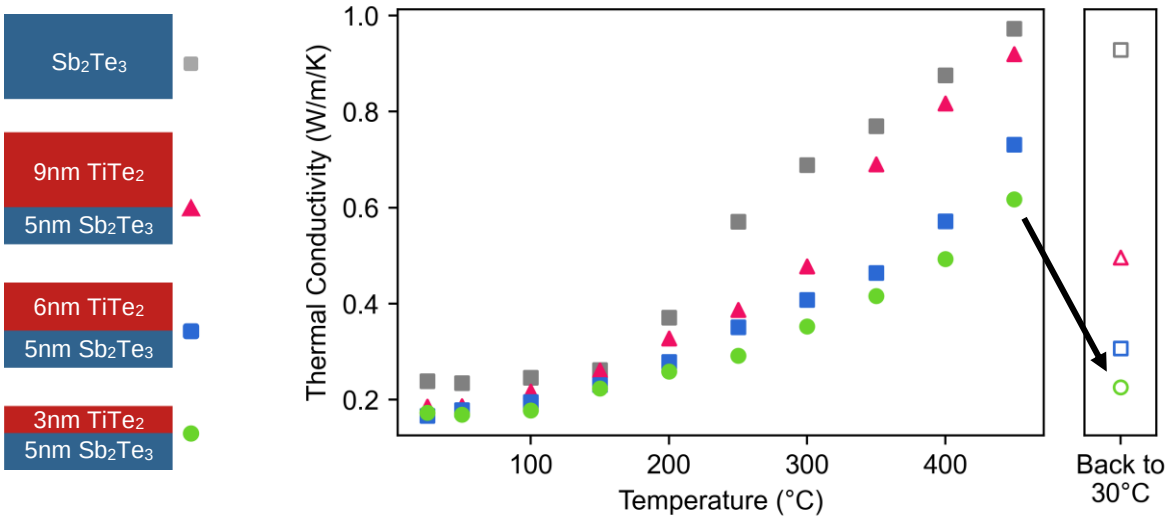

Fig. 4: Three types of superlattices are compared to bulk Sb_2Te_3 during *in situ* TDTR measurements. Thermal conductivity increases for all samples when heating up. After cooling down the 5-3 superlattice still shows a very low thermal conductivity, despite its crystallinity.

Investigation of superconductivity in ultrathin PtSi films formed by employing a novel self-alignment process

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Schottky barrier (SB) transistor is used in a variety of applications. Recently, Platinum silicide (PtSi) has been investigated as the metallic source and drain terminals of SB metal-oxide-semiconductor field-effect transistors in cryogenic CMOS as well as in quantum bits (qubits) based on nanoscale Josephson field-effect transistors (JoFETs) [1]. The formation of superconducting PtSi film usually starts from physical vapor deposition (PVD) on a precleaned silicon substrate of a platinum layer, followed by rapid thermal processing (RTP). The superconductivity in ultrathin PtSi films formed by employing a novel self-aligned process, i.e., thermal oxidation and selective removal of unreacted Pt in aqua regia after silicide formation [2], is characterized in the present work. Although severe agglomeration of the 3.1 nm thick PtSi film after the thermal oxidation at 600 ^{o}C is observed (Fig. 1), the superconductivity prevails with a higher critical temperature (T_C) than that of its precursor as-formed film at 500 ^{o}C (Fig. 2). Rutherford backscattering spectrometry (RBS) was employed for Pt thickness calibration while grazing incidence X-ray diffraction (GIXRD) for both confirmation of the PtSi formation and estimation of the PtSi grain size according to the Scherrer equation (Fig. 2). The continuous increase in T_C could be correlated to the monotonous increase in average grain size when the PtSi film thickness increases for both as-formed and oxidized films. Of special interest is the doubling of the estimated average grain size (thickness) in the oxidized sample with 3.1 nm PtSi, which fits well with the estimated severe reduction of surface coverage by 50% (Fig. 1) of the agglomerated PtSi film. The results clearly indicate that T_C is governed by the property of the best percolating path in a superconducting film. Furthermore, new process solutions to mitigating the agglomeration of sub-5 nm thick PtSi films have been developed.

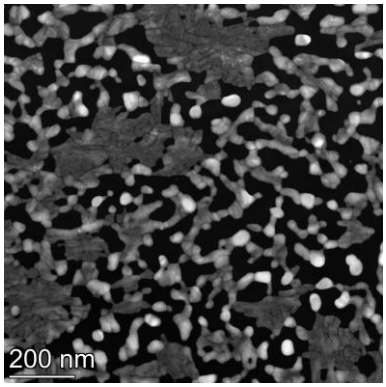

Fig. 1 Plan-view, high-angle annular dark field (HAADF) TEM image for a 3.1-nm PtSi sample after sequential RTP in N_2 at 500 °C for 30 s and in O_2 at 600 °C for 60 s [2]. Bright parts are PtSi while dark parts are exposed Si.

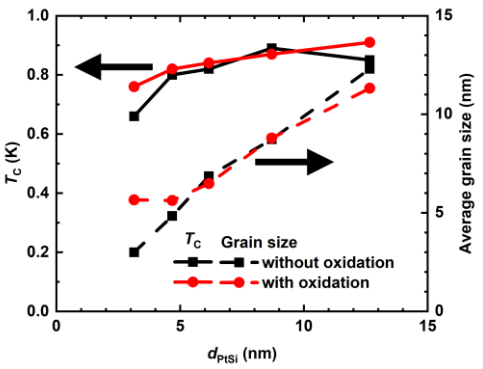

Fig. 2 Critical temperature, T_C, and average grain size as a function of PtSi thickness, d_{PtSi}, for PtSi films formed at 500 °C with or without subsequent thermal oxidation.

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Carrier profiles measurements on 4H-SiC MOSFETs by Scanning Spreading Resistance Microscopy and Scanning Capacitance Microscopy

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New generation of silicon carbide (4H-SiC) metal oxide semiconductor field effect transistors (MOSFETs) are increasing their performance in terms of On-resistance (RON), and maximum operating current also by shrinking of the cell-pitch and optimized thermal activation of the implanted regions [1]. In 4H-SiC MOSFETs, ion implantation is a very powerful technique to introduce dopand species (n-type: Phosphorous and p-type: Aluminium) in specific regions of the semiconductor, this process is followed by high-temperature annealing for the electrical activation [2,3]. As matter of fact, the designed doping level is chosen by TCAD simulation of the final device structure. However, a nanoscale measurement is needed to understand the real device performance, both the active doping concentration (or the material resistivity) and the real device geometry (e.g. size of the implanted region, junction depths, etc.).

In this context, two dimensional (2D) electrical scanning probe techniques (SPM), such as scanning capacitance microscopy (SCM) and scanning spreading resistance microscopy (SSRM), can give useful information both on the spatial distribution of the active dopants concentration and local resistivity in the region underneath the tip [4]. The SCM and SSRM have been widely employed for quantitative 2D carrier profiling in silicon-based CMOS structures [5]. Conversely, while there has been extensive exploration of the potentials of SCM [4] and SSRM [6] on wide bandgap semiconductors, there remains a necessity for focused endeavours to evaluate their 2D profiling capabilities. Specifically, a more in-depth investigation is required into the current injection mechanisms at the contact point between the SPM tip and 4H-SiC, aiming for a comprehensive quantification of the SSRM map. However, the complementary use of SCM and SSRM on identical device structures can provide precious information eventually on the discrepancy between the designed and the real device.

In this paper, SCM and SSRM analyses have been performed on the channel region of a vertical 4H-SiC power MOSFET, with the aim to determine the n-type and p-type distribution in real device, and to estimate the lateral resolution of these two complementary SPM methods and their capabilities on the detection of doping level variation across the unitary cell.

Fig. 1 shows the TCAD simulated structure of the planar power MOSFET in cross section, where two different cut lines are reported to estimate the free carrier concentration across the channel and the JFET regions.

Figs. 2a, 2b and 2c show, respectively, the AFM morphology, the SCM and the SSRM maps collected using conductive diamond coated Si tips on a MOSFET device, prepared with a bevel angle of 5° 44', giving rise to a 10× magnification in the vertical direction. As can be noticed, the SCM image, based on local differential capacitance (dC/dV) measurements, is very sensitive to the majority carrier variations in the JFET depletion regions. On the other hand, the SSRM image, based on resistance measurements by a logarithmic current amplifier, shows clear signal variation in the gate region. To better illustrate the SSRM sensitivity and lateral resolution, the measured resistance across the gate insulator region is depicted in Fig,3. As can be noticed, an abrupt resistance variation across the SiO2/4H-SiC interface is detected. This information can be used to determine the lateral spatial resolution (from the 10% to 90% signal variation) of about 5 nm (red box in Fig. 3).

A quantification of the measured resistance maps to local resistivity requires a deeper understanding of the mechanisms of current injection from the conductive tip to the differently doped 4H-SiC MOSFET regions. To this aim, local current-voltage (I-V) characteristics were collected by the SSRM logarithmic current amplifier on a single point in the Drift, Body and Source regions, as shown in Fig. 4. The I-V collected on the drift and body regions are compatible with a forward n-type and reverse p-type Schottky-like conduction. On the other hand, the I-V collected on the source region shows a current value 4 orders of magnitude larger, compatible with current injection by thermionic field emission. Differently than for SSRM measurements on Si samples, where Ohmic contact formation between the tip and the semiconductor was achieved by applying a sufficiently high force, a non-linear behavior of I-V curves is observed on both p- and n-type doped 4H-SiC, even on the highly doped source region. Hence, both the tip/SiC contact and spreading resistance contributions must be considered to appropriately describe current injection in 4H-SiC, in order to make a quantification of SSRM signal to resistivity map.

Even though this aspect deserves further investigation, SSRM is promising for the investigation of shrunk latest MOSFETs generation in terms of lateral resolution.

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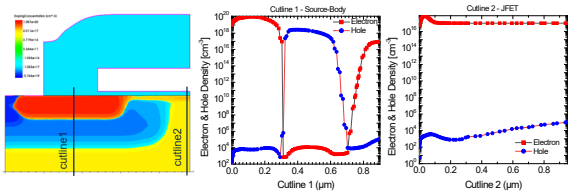

Fig. 1: TCAD free carriers simulation across the unitay cell in an ideal MOSFET.

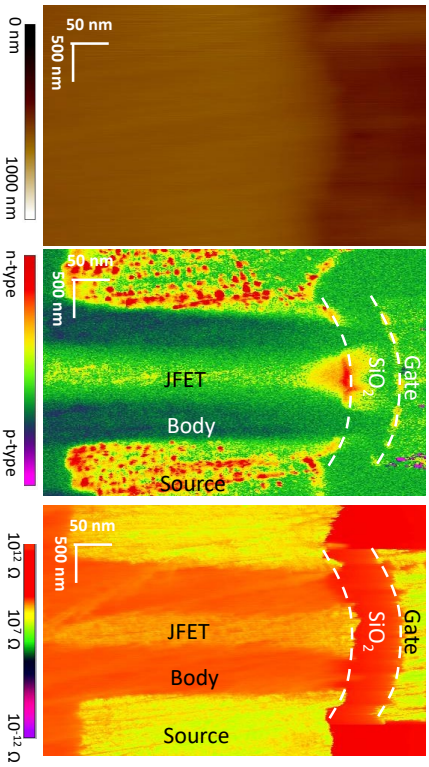

Fig. 2: (a) AFM morphology, (b) SCM and (c) SSRM signals.

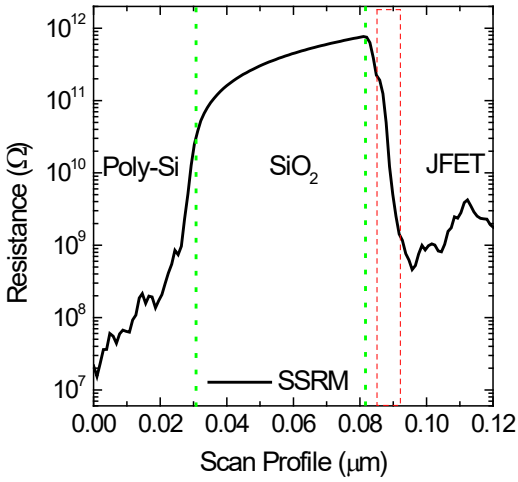

Fig. 3: SSRM profile across the gate insulator region.

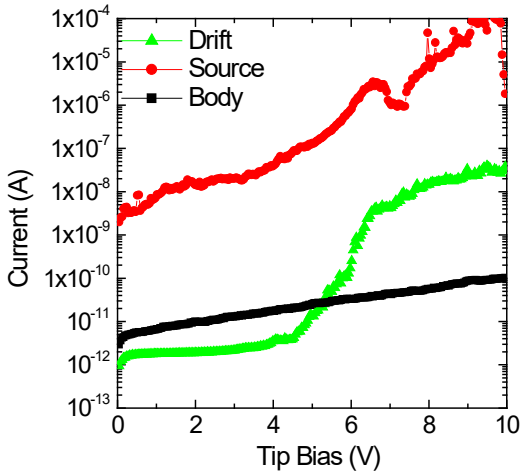

Fig. 4: Local I-V curves extracted from the SSRM signal in the Drift, Body and Source regions.

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Electrical performances of Tantalum Nitride Thin Film Resistors (TFR) versus N-content modulation

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Nowadays, precise thin film resistors (TFRs) play a fundamental architectural role in advanced semiconductor power devices, in order to target higher stability, accuracy, and reliability, as well as lower noise for high-precision applications, such as electronic measuring systems, monitoring equipment, audio applications, precision controls and instrumentation.
High resistivity and good thermal stability are crucial properties for the realization of a TFR. Besides well-established alloys such as SiCr or NiCr, another performing class of materials for the purpose is tantalum nitrides (TaN). TaN is known to have a complex diagram phase, forming different stable and metastable phases [1,2], and this leads to a considerable variation in its electrical properties upon deposition conditions and process parameters, such as N_2 partial pressure or temperature during sputtering, because they directly impact on chemical composition and structure of TaN films.
In this work, constant-pressure reactive DC magnetron sputtering was used to produce TaN thin films employing tantalum metallic target, nitrogen as reactive gas, and argon as plasma-supporting gas. A set of five different films was obtained by varying N_2 flow, ranging from 0 to 20 standard cubic centimeters (sccm). The corresponding electrical properties of these films were investigated: the sheet resistance of the films increases with nitrogen content, in a range between 75 and 1000Ω/□, while the temperature coefficient of resistance (TCR) spans four order of magnitude, between -10^3 and +10 ppm/ºC (Fig. 1). TCR expresses resistance variation with temperature: a positive value implies that the resistance of the material increases with a temperature increase, while a negative TCR means that the resistance decreases by increasing the temperature. The ideal condition for high-performance devices is to have temperature-independent resistance. This condition is approached by the new-studied low-nitride TaN (5sccm N_2), exploiting the opposite contributions of Ta (+TCR) and Ta-N (-TCR), which allow to achieve a compensation, thus reaching a near-zero TCR value [3].
For the electrical characterization, the study concurrently carried out the integration of all the investigated TaN films in the front-end-of-line of advanced BCD technology on 200mm wafers. The films were integrated upon an oxide layer and capped by silicon nitride to prevent oxidation, providing versatility to be implemented into different modules both in front-end-of-line (FEOL) and within the metallization layers of the back-end-of-line (BEOL). Patterning of these layers was conceived as fully compatible with every N-content layer, employing a single dry etching strategy in combination with a dedicated wet removal to avoid Ta-polymer residues. For TaN etching, a chemistry in BCl_3, Cl_2, and Ar with good selectivity towards underneath oxide was employed, combined with a wet removal with SPM (H_2SO_4 : H_2O_2) and SC1 (NH_4OH : H_2O_2 : H_2O).
The results showed that the new TaN film at low nitride content provided the most promising electrical performances for the required scope. By full integration of TaN films on power components of advanced BCD devices, excellent stability with temperature was proven, reaching a TCR of approximately 150 ppm/ºC and a sheet resistance of 75 Ohm/□, making it an adequate solution for TFR realization. To target higher electrical performances and to approach those of the major competitive materials, such as SiCr or NiCr, further retuning is possible by properly targeting the nitrogen flow and modulating the film thickness to reach higher sheet resistance values. In addition, the single-integration strategy guarantees an easy-to-integrate and manufacturable solution according to device requirements.

Keywords: tantalum nitride (TaN); thin film resistor (TFR); sheet resistance, temperature coefficient of resistance (TCR)

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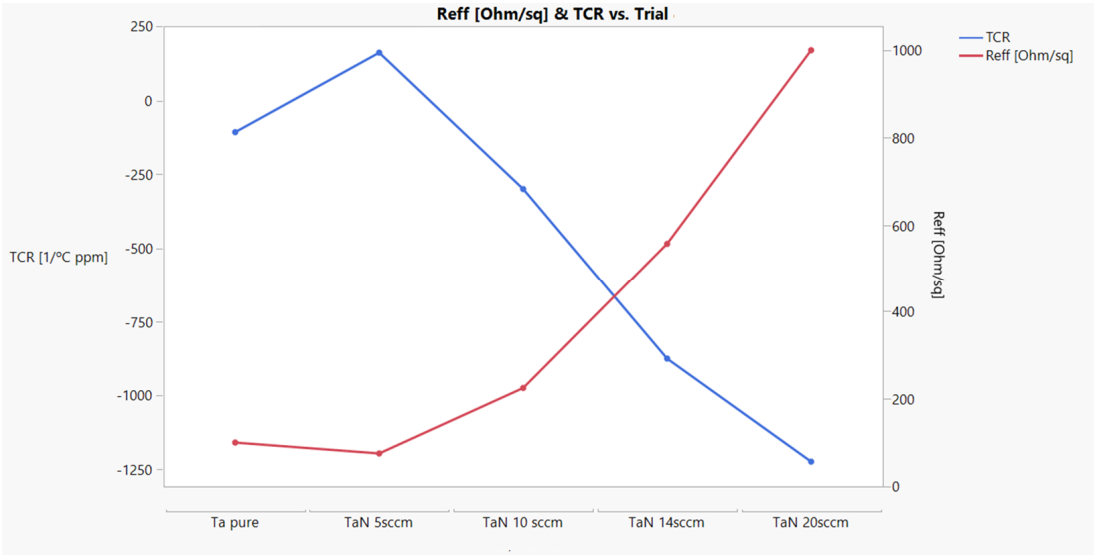

Figure 1 – TaN sheet resistance (red) and TCR (blue) modulation with N_2 flow

Characterization of Molybdenum Oxide: Understanding Growth Kinetics and Molybdenum Consumption for Materials Science Applications

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The natural tendency of molybdenum to oxidize with the subsequent thinning of molybdenum layer is an important factor to be considered during the process flow of micromachined devices. The characterization of molybdenum oxide has revealed important findings regarding its behaviour and properties.

The phenomenon has been studied on two different samples. A thin layer (2000Å) of molybdenum has been deposited via magnetron sputtering using Evatec Clusterline on oxidized silicon substrates. One of these samples has been treated with a customized wet cleaning process and the second not. The presence and the kinetic of molybdenum oxide growth have been evaluated using ellipsometry (KLA ASET-F5x), surface resistivity (CDE ResMap Four Point Probe Resistivity Mapping System), XRD (Bruker JVX7300L) and TEM analysis. The thickness of molybdenum oxide measured by ellipsometry was found to be strongly dependent on surface treatments. After almost 60 days, molybdenum oxide thickness was 30 Å for untreated surface and 15 Å for the treated one [Fig 1]. The accuracy of the ellipsometric measurement has been validated by TEM analysis on tween samples, as shown in [Fig 2]. The oxidation process seems depending by a rather complex kinetics, showing a fast linear grown phase in the first ten/twenty days from deposition, depending by the surface treatment, followed by a slowdown of the growing rate. Assuming MoO_3 as the only species formed during the oxidation, from a stoichiometric evaluation, the consumption of molybdenum for a given layer of molybdenum oxide is approximately one third of the oxide thickness.

The growth kinetic of molybdenum oxide appears to be influenced by the chemical treatments of the metallic layer. The treatments with alkaline cleaning solutions have a passivation effect on the metal surface, influencing the total amount of oxide formed as well as the kinetic of oxidation. Sheet resistance measurements, slightly changing with time, shows an average higher resistivity of treated surface supporting this hypothesis [Fig. 3].

The results of this study provide valuable insights into the behaviour and properties of molybdenum oxide, which can be useful for various applications in the field of materials science. The observed non-uniformity in oxide thickness and the consumption of molybdenum due to oxide growth are critical considerations for the design and fabrication of MEMS structures. The influence of metallic layer thickness, morphology, and chemical treatments on the growth kinetics of molybdenum oxide highlights the importance of carefully control these parameters in MEMS fabrication.

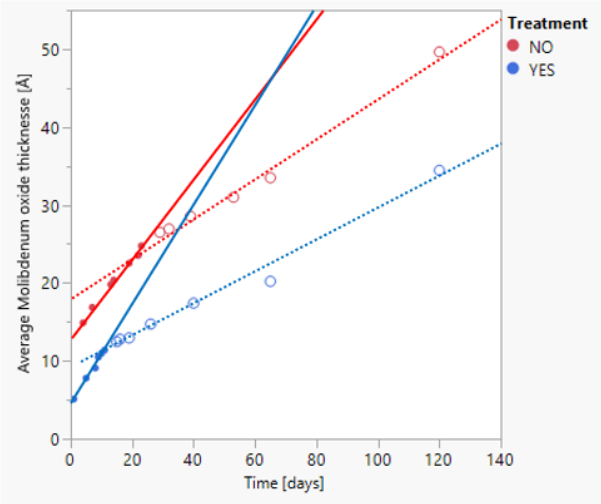

Figure 1. Ellipsometric measurements of molybdenum oxide along 120 days from deposition. Treated surface (blue) and not treated surface (red). Points refers to the average of 49 points measured on wafers. Solid and empty points refer to fast and slow kinetic phase respectively while solid and dotted lines are the respective linear trends.

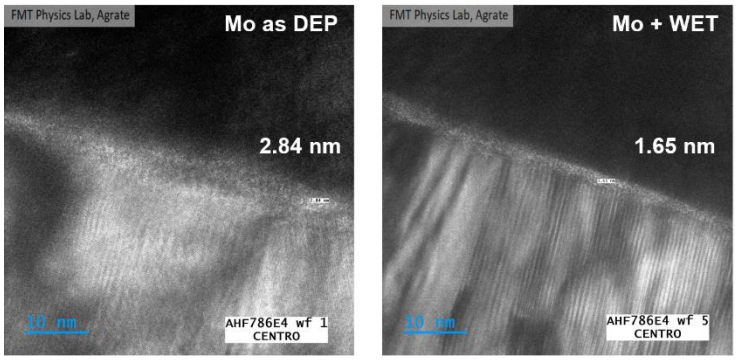

Figure 2. TEM images of molybdenum oxide after 60 days from deposition. Treated (Right) and not treated (left).

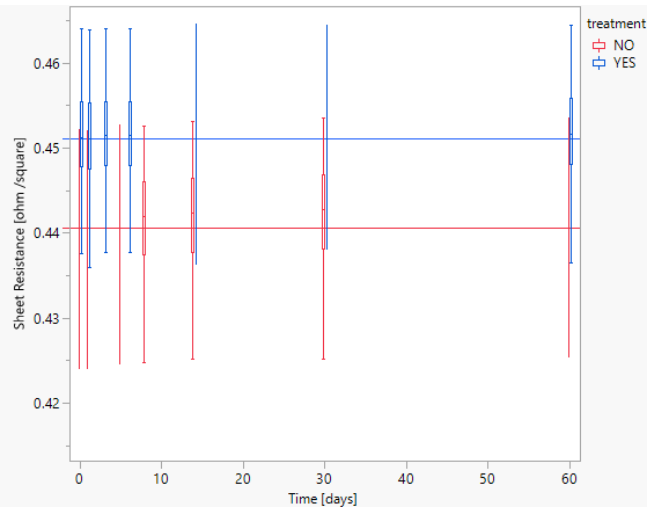

Figure 3. Surface resistivity measurements of molybdenum oxide along 60 days from deposition. Treated surface (blue) and not treated surface (red). Boxplot refers to the 49 points measured on wafers while solid lines refer to data average values.

Cantilever test structures for stress characterization in multilayer MEMS membranes

Federica Capra[a*], Angelica Baldini, Matteo Bisogni, Chiara Carra, Filippo Daniele, Filippo D'Ercoli, Marco Dosi, Silvia Nicoli, Mattia Pallaro, Andrea Taini, Lorenzo Tentori, Igor Varisco

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Residual stress of thin films is a critical aspect which has to be carefully taken into account during both design and manufacturing of MEMS sensors and actuators.
In this respect, it's extremely important to understand the mechanical behaviour of MEMS membranes where a specific deflection can directly impact the MEMS device performance.

The stress of one or more films that are composing a moving membrane cannot be measured by conventional stress characterization approaches.
In this work, a method to extrapolate the residual stress of a multilayer MEMS membrane has been evaluated. This technique is based on the characterization of an array of cantilevers test structures which are fabricated on silicon wafers employing a simplified MEMS process flow.
Upon release, the cantilevers deflect to partially relieve the unbalanced residual stress in the thin films. Visible light interferometry is employed to quantify the deflection of the cantilevers, allowing for the calculation of residual stress in all the integrated thin films.

The deformation profile of the cantilevers test structures (Fig 1) has been measured by interferometry on Rudolph Technologies NSX 330 26 sites per wafer. By matching the measured displacement and the simulated one, residual stress has been reconstructed through finite-element analysis (FEA) with COMSOL Multiphysics® (Fig 2).

The output of this work is to provide the fundamental mechanical information of the multi-stack layer needed to properly assess the design and the validation of the MEMS membrane. The ability to probe local stress variations (Fig 3) opens up new opportunities for stress analysis in multi-layer stacks, which are prevalent in complex MEMS structures. The proposed method provides also a valuable tool for optimizing the connection between MEMS design and fabrication phases.

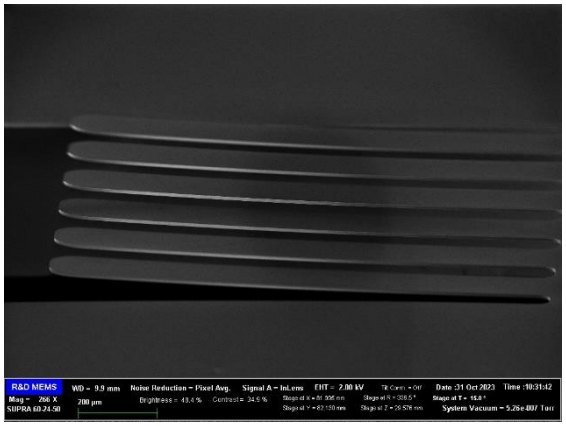

Figure 1. SEM image of released cantilever test structures.

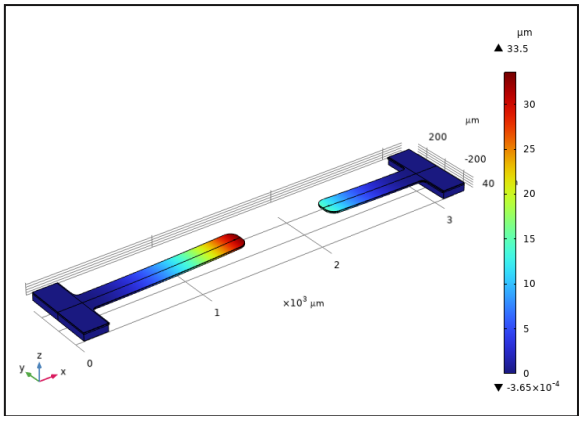

Figure 2. Cantilever test structures simulation, out-of-plane displacement.

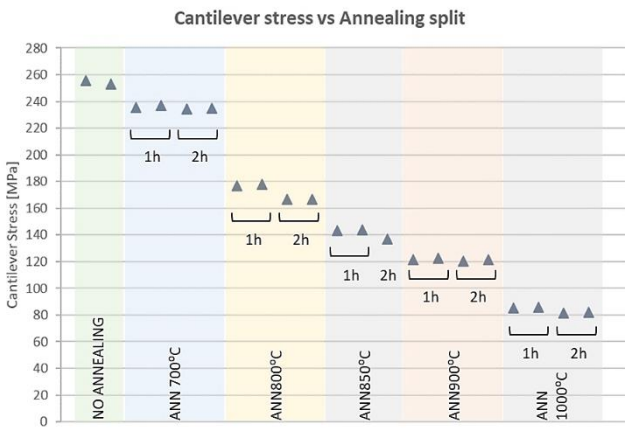

Figure 3. Cantilever stress trend as a function of thermal budget.

Extra pattern defectivity formation due to silicon oxynitride interaction with DUV Photoresist during pGaN gate patterning for HEMT device

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pGaN gate definition is one of the key process steps for HEMT Power GaN device fabrication. Particular attention should be paid during the patterning module to avoid the presence of defects that could be responsible for electrical failures. This study is focused on extra pattern defects that were observed at the in-line inspection after pGaN etch process step. The mechanism behind defect's formation and both the morphological and electrical impact will be explained. Finally, a possible integration flow that ensures the absence of these extra patterns will be described.
The physical characterization (TEM and EDX analyses) showed the presence of pGaN residues, arranged either in line or found as "grapes" agglomeration close to pGaN.
The extra patterns present over AlGaN can hide other types of defects saturating the defectivity maps. Also, reliability failures have been found and correlated with this type of defectivity.
A step-by-step analysis was carried out to define the mechanism of defects formation and the root cause. The patterning process makes use of a DUV (deep UV) photoresist and proceeds through three main steps: etching of the oxide hard mask (HM), stripping of the photoresist, etching of pGaN. The analysis, reported in Fig. 1, shows that defects with the same shape of the extra patterns were already present after the HM etch step. One of the hypotheses about this micro masking effect was the presence of photoresist residues above the oxide defects. These residues could have been generated by the interaction between the DUV photoresist and the oxide during the exposition of the mask. The hard mask is a TEOS layer prepared by means of Plasma Enhanced Chemical Vapor Deposition (PECVD) technique. After TEOS deposition, a layer of silicon nitride is deposited by Low Pressure Chemical Vapor Deposition (LPCVD) in ammonia ambient. This Si_3N_4 layer is subsequently removed from wafer front through a plasma etching. Time of Flight Secondary Ion Mass Spectrometry (ToF SIMS) analysis of the oxide showed a high component of SiN_x at the surface, meaning that the layer was partially converted into an oxynitride film. It's reported in literature that silicon oxynitride films are incompatible with DUV photoresist. The reactive nitrogenous species diffuse out of the oxide layer and chemically interact with the components of the polymeric material of the resist [1]. Amine radicals are known to neutralize the acid catalyst of such type of photoresist [2].
A solution was adopted to avoid any interaction between the oxynitride film and the photoresist material. With the new integration the extra patterns defects were eliminated and, regarding reliability, a large improvement in time to failure has been observed.

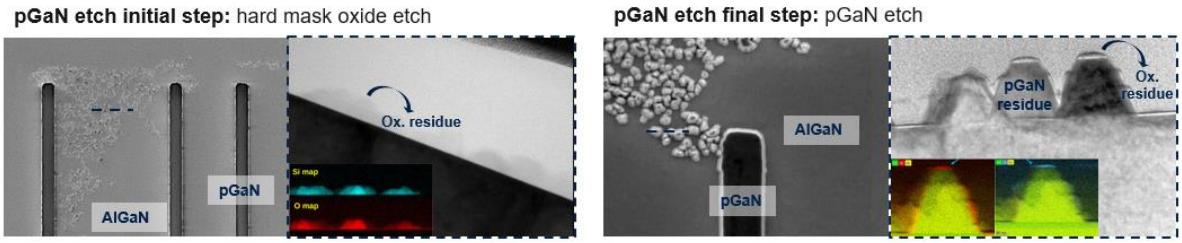

Figure 1 – SEM top view and TEM cross section of extra pattern defectivity formation above AlGaN during pGaN etch step.

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In Vacuo XPS Study of Al_2O_3 Atomic Layer Deposition on GaN

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Vertical GaN-based switching transistors are currently receiving increased attention as an alternative to Si and SiC-based devices. GaN-based metal insulator semiconductor field effect transistors are among the most promising vertical power switching transistor architectures.[1] For secure typically OFF operation, a broad gate positive voltage span and a stable threshold voltage, reliable gate insulators are needed. For this reason, an Atomic Layer Deposited (ALD) Al_2O_3 layer with a relatively high permittivity, large band gap, and high breakdown electric field is often used as a gate insulator. Jackson *et al.*[2] demonstrated that different wet surface treatments of GaN prior to Al_2O_3 ALD influence the chemical composition and affect the electrical device performance. In this work, *in vacuo* X-ray Photoelectron Spectroscopy (XPS) is used to study the GaN surface composition after plasma pre-treatment and after the initial ALD cycles for both thermal (using water as precursor) and plasma-enhanced (using O_2-plasma) ALD growth of Al_2O_3 onto GaN, without exposing the sample to air.

First, the effect of a plasma treatment prior to ALD is investigated. Both NH_3- and H_2-plasma pre-treatment can successfully remove spurious C-contamination from the pristine GaN surface while a heat treatment at 400 ºC alone is not sufficient (Fig. 1). In addition, only NH_3-plasma is found to remove a large fraction of the O-species that are present on the pristine GaN surface. After the first ALD-half cycle i.e. after exposure to trimethylaluminium (TMA), the signal of the Al2p and C1s XPS spectra are found to increase which is consistent with the adsorption of TMA to the surface (data not shown here). This observation demonstrates the in vacuo XPS method is sensitive to detect the growth of a signle (sub)monolayer of TMA on the surface. During the second ALD half-cycle, the TMA treated surface is exposed to water (thermal ALD) or O_2-plasma (plasma-enhanced ALD process). In both cases, the data (Fig. 2) is consistent with the growth of Al_2O_3. Water exposure is found to offer insufficient reactivity to remove all of the adsorbed TMA ligands from the surface, while O_2-plasma removes all detectable C. Further it is observed that the O concentration in the near-surface region increases dramatically after O_2-plasma exposure, coinciding with the formation of O-Al, O-Ga and NO-Ga species on the surface.

Electrical data show that the density of trap states is lower for the NH_3-plasma treated samples, which seems to correlate to the enhanced removal of Ga_xO_y of the pristine GaN surface.[3] In addition, more trap states were observed for samples deposited using the thermal ALD process, likely related to the presence of C-impurities, caused by the incomplete removal of the TMA ligands by water as detected by XPS. For the plasma-enhanced ALD process more hysteresis is observed between the forward and reverse bias stress sweep CV cycles, indicating a high content of stress indued interface traps. This might be explained by the presence of O-defects created during the O_2-plasma pulse. The best electrical data were achieved when combining a NH_3-plasma pre-treatment, followed by initial Al_2O_3 growth using thermal ALD, and then switching to plasma-enhanced ALD to thicken the Al_2O_3 layer.

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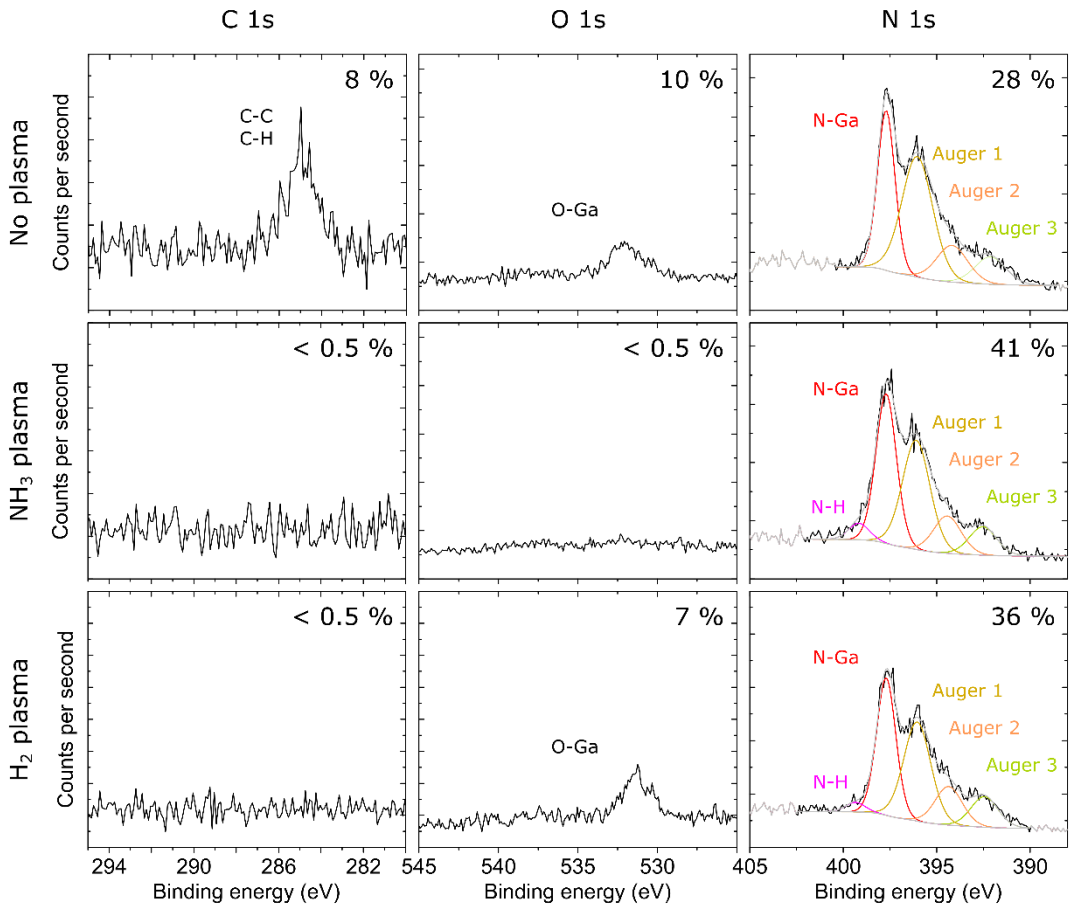

Figure 1 In vacuo XPS spectra acquired after heat pre-treatment and no plasma (top), NH_3-plasma (middle) and H_2-plasma (bottom) of a n-GaN surface.

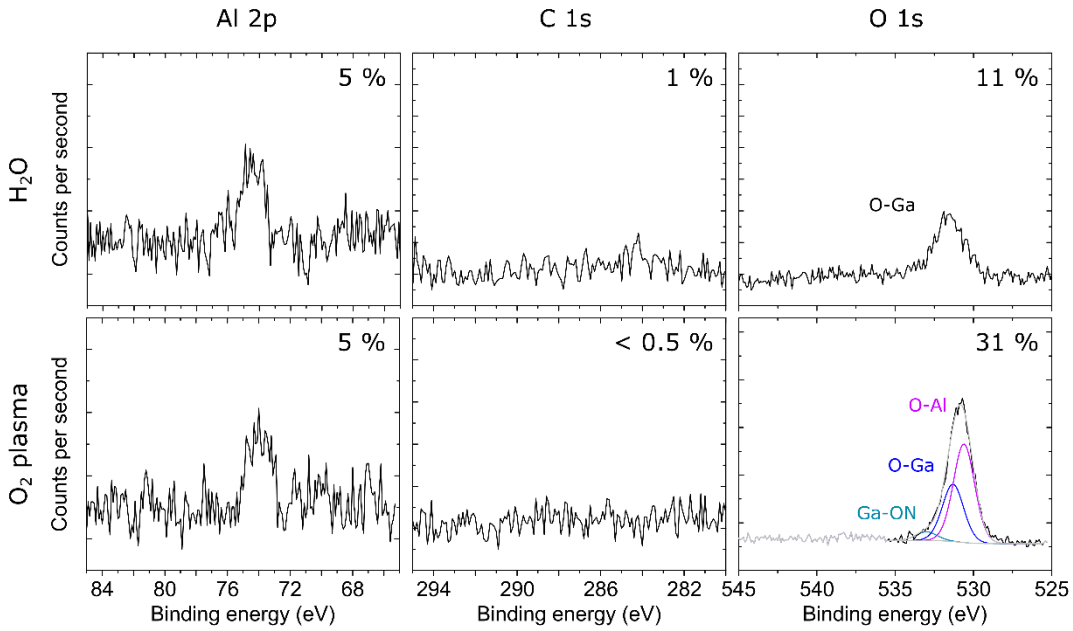

Figure 2 In vacuo XPS spectra acquired after water exposure (top) and O_2-plasma (bottom) during respectively the thermal and plasma-enhanced Al_2O_3 ALD process on a H_2-plasma pre-treated GaN surface.

Mechanical Properties and Evidence of Asymmetrical X-Ray Diffraction Peak Broadening in Crystalline $Ge_2Sb_2Te_5$ Thin Films

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Te-based chalcogenides materials gathered a high interest because of their increasingly important role in the technological applications. Indeed, in the last decades they have been adopted in non-volatile memory devices as replacement of traditional charge trap technologies [1-3]. Phase-Change Memory or "PCM" technology bases its functionality on the reversible phase transition of a chalcogenide alloys between an amorphous and a crystalline phase, induced by an electrical pulse, leading to a huge change of the electrical resistivity into the device. This allows storing two or more "bits" in a single memory cell [4]. Among all the different types of emerging memory technologies, PCM was the first one to reach the volume production proving its already high maturity. Furthermore, PCM recently achieved the highest level of reliability (i.e. grade 0), demonstrating its suitability for the embedded automotive market [4-5].

A wide variety of phase-change materials have been already studied, however $Ge_2Sb_2Te_5$ (GST) remains the most studied material because of its congruent nature and its key role in more complex alloys [6]. Prototypical GST presents a stable stoichiometry, without atoms diffusion or phase segregation during the amorphous to crystalline phase transition. Under thermal annealing, amorphous GST first crystallizes into a face-centered cubic (f.c.c.) phase (space group: Fm-3m). During this phase transition, a density increase and a thickness reduction have been observed in several references [8-8]. This volume shrinking results in the build-up of a significant tensile stress.

XRD is the best-suited characterization technique to investigate strain and microstrain by a microstructural point of view. Complementary to TEM, XRD give an average characterization on a large sample volume with relevant grain statistics and has a very high resolution in the reciprocal lattice. Sensitive strain effects are the observable on X-ray diffraction (XRD) patterns, such as peaks shifts (macroscopic strain) and peaks broadening (microscopic strain).
More generally, X-ray diffraction peaks broaden when the crystal lattice becomes imperfect. According to the theory of kinematical scattering, peaks broadening, characterized by the Full Width Half Maximum (FWHM) of the diffraction peaks, originates from small crystallites size effects and/or if lattice defects (heterogeneity, microstrain, gradient) are present in enough large abundance.

Extensive studies have already been conducted on chalcogenide materials using XRD, however full, consistent, fine and deep studies of line profiles in crystalline f.c.c. GST films has not yet been reported.

In this work and for the first time, thermally crystallized f.c.c. GST thin films are studied by X-ray diffraction through multi-{hkl} reflection, at different tilt directions of the film (**Fig. 1**) and focused on peaks positions and line profiles broadening.
Consistent, full and deep investigations are carried out, to give new insight on the mechanical state of crystalline cubic $Ge_2Sb_2Te_5$. This full large Reciprocal Space Mapping and deep data analysis allow to deduced the X-Ray Elastic Constant (XEC). In addition and as special focus, an atypical asymmetric line profile broadening (or peak shape) of Bragg peaks is also observed and discussed, with the support of instrumental and material considerations.

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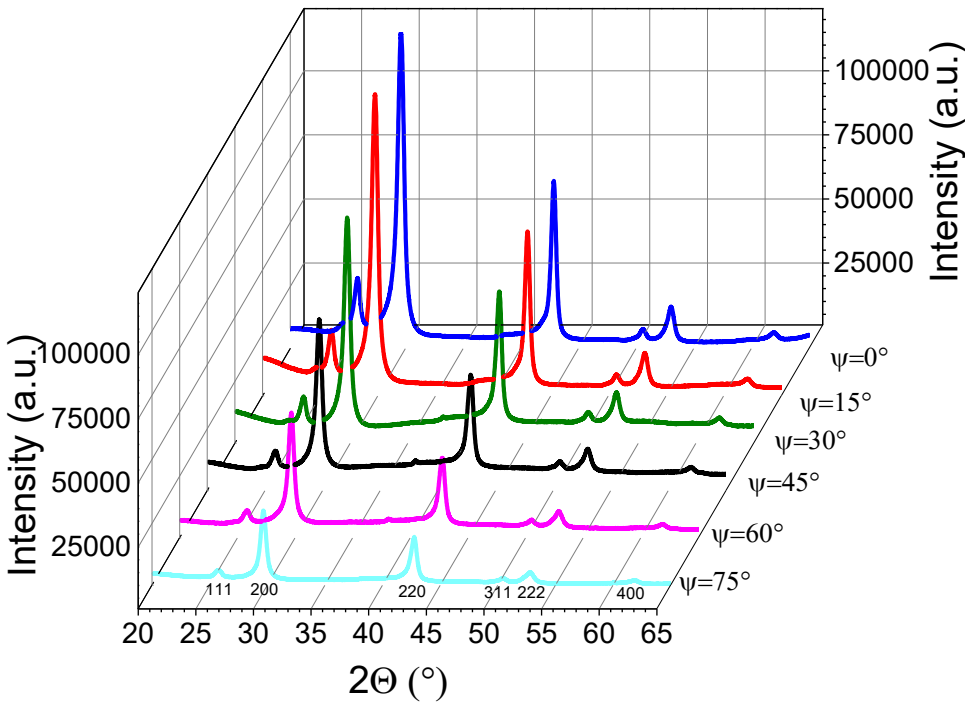

Fig. 1: θ-2θ scans at different tilt angle (Ψ) for the thermally crystallized GST sample. The {hkl} reflections are indexed and correspond to the f.c.c. GST phase. All the same {hkl} reflections are observable at the different Ψ angles. By fitting the Bragg peaks, 2θ positions and FWHM are determined for all the different {hkl} planes and different tilt (Ψ) angles.

Influence of the annealing schemes and silicide thickness on the stability of Ni(Pt)Si thin film formed on 300 mm Si(100) wafers

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Nickel silicides, due to their low resistivity and low formation temperature, are today used in the microelectronics industry to ensure electrical continuity between tungsten contacts and transistors for advanced technology nodes, below 65 nm [1]. Nevertheless, the emergence of new FDSOI technologies (for Fully Depleted Silicon On Isolator) induces a drastic reduction of Ni(Pt)Si final thickness, and then, a higher sensitivity to agglomeration [2,3]. To prevent such degradations in the case of 3D integrations, recent studies reveal that the annealing schemes might influence the thermal stability of final Ni(Pt)Si layer, in particular partial anneal seems to present real advantages in terms of thermal stability [3,4]. In addition, based on the work of T. Luo at al. [5]; Si diffusion at Ni(Pt)Si/ Si interface appears to be the most influent factor in agglomeration phenomena, and final species distribution might indicate the progress in agglomeration stages.

We propose in this paper a systematic study of the influence of annealing schemes (partial, total and unique anneal) on Ni(Pt)Si films thermal stability for different final thicknesses (14, 20 and 24 nm, as described in Fig. 1). To explore the film agglomeration evolution, all samples are submitted to additional anneals at a temperature comprised between 550 and 800 °C for 30 s (Fig. 1). In this way, several ex-situ characterization techniques (4-point R_s, tilted-SEM, TEM-EDX, ToF-SIMS) have been used to identify morphological and chemical evolutions inside silicide layer, and also at interfaces (silicide top surface and Ni(Pt)Si/Si interface mainly).

Rs and tilted SEM characterizations for all studied samples are shown in Fig. 2. In details, for a final thickness of 14 nm, morphological degradation is observed at 600 °C for total and unique anneals contrary to partial anneal (Figs. 2a,d). This delay in agglomeration phenomenon linked to partial reaction is not so clear for 20 and 24 nm. For thicker films, all anneal schemes appear to be almost equivalent (Figs. 2b,c,e,f). Nevertheless, the agglomeration temperature is shifted to the high temperatures for thicker silicide films (here 700 °C), as expected. And a slight delay in agglomeration stages is then observed for unique anneal. One might observe a clear threshold in thermal stability between 14 and 20 nm like " a frontier", as already proposed by F. Geenen et al. [2]. TEM cross-sections obtained after the formation of 14 nm-Ni(Pt)Si by partial, total and unique anneal and an additional anneal at 550 °C are shown in Fig. 3. Such observations allow to clearly identify the starting point of agglomeration, usually called grain boundary grooving, in the case of a total anneal at 550 °C (Fig. 3b). In addition, EDX profiles obtained perpendicularly to the Ni(Pt)Si layers for all samples are displayed in Fig. 4. We focused here on Pt redistribution at the top surface, inside silicide layer, and at the interface between Ni(Pt)Si film and Si substrate. Significant differences in Pt redistribution are observed for 20 nm-Ni(Pt)Si layers (Fig. 4b). Higher Pt concentrations are detected for partial, and total anneals at Ni(Pt)Si/Si interface compared to unique anneal treatment. This could be an indication of higher Pt diffusion through silicide grain boundaries during the first stages of agglomeration in this case relating to a change in grain size or grain boundaries orientations. Moreover, we could highlight that the Pt atomic concentration increases at the top surface of silicide films increase consistently to the silicide thickness (as an example for unique anneal, from 8 to 12 at.%, Figs. 4a, b and c). Thus, the delay in agglomeration phenomenon for Ni(Pt)Si films could be not only related to silicide film thickness, but also to higher concentration of Pt at the interfaces which moderates the Si diffusion.
In the final paper, additional characterization and deep discussions on the influence of anneal schemes and silicide film thickness will be exposed to identify the role of minor species distribution on Ni(Pt)Si thermal stability.

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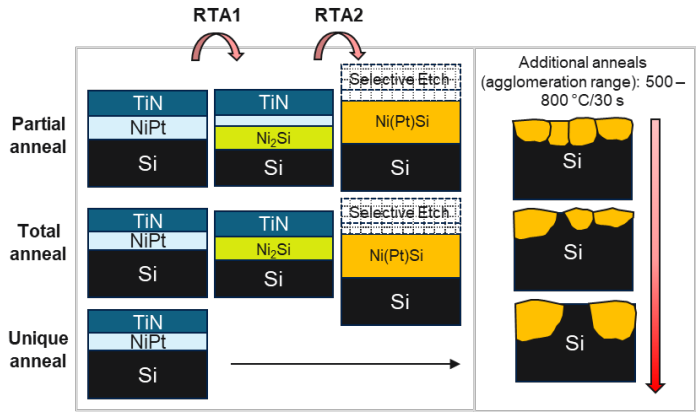

Fig. 1: Process flow used, based on the salicide process, to form different thickness of Ni(Pt)Si layers.

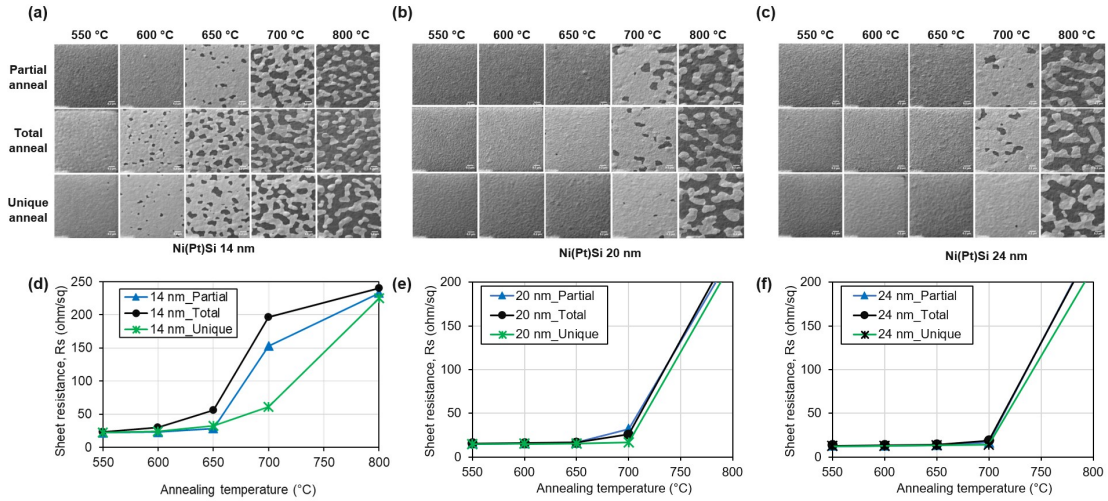

Fig. 2: Top-view tilted-SEM images of Ni(Pt)Si films presenting different final thicknesses equal to (a) 14, (b) 20, and (c) 24 nm formed by total, partial and unique anneal. Tilted-SEM images are correlated with R_s resistance measurements displayed in d, e, and f respectively for each Ni(Pt)Si thickness.

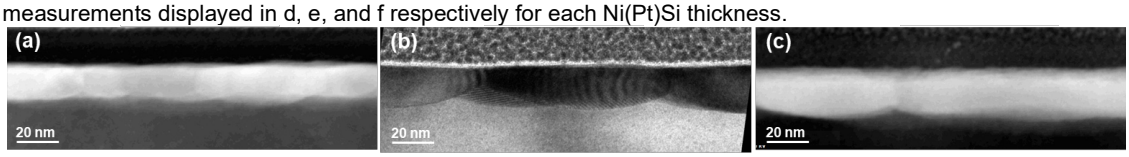

Fig. 3: Cross-section TEM images of 14 nm Ni(Pt)Si films formed by (a) partial, (b) total, and (c) unique anneal after an additional anneal at 550 °C for 30 s. Grain boundaries grooving is clearly observed for total anneal indicating the early stages of agglomeration.

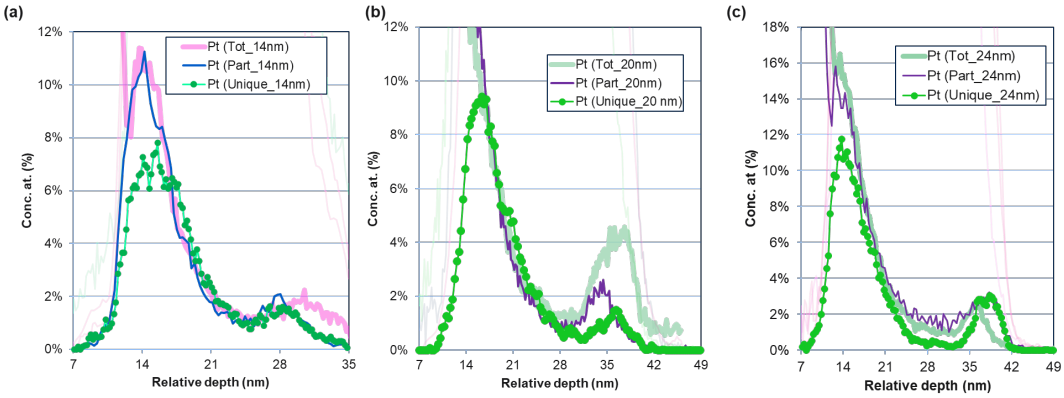

Fig. 4: TEM-EDX line scans describing the Pt redistribution within the (a) 14, (b) 20, and (c) 24 nm Ni(Pt)Si layers formed by partial, total and unique anneal, and an additional anneal at 550 °C for 30 s. Pt accumulations are then observed at top surface of Ni(Pt)Si film and Ni(Pt)Si/Si interface.

Study on surface modification of recycled carbon fiber to improve interfacial bonding strength with thermoplastic resin

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In this study, carbon fibers recovered from waste carbon composites were subjected to chemical desizing, surface treatment, and resizing (Fig.1) for the purpose of upcycling, and the changes in mechanical and chemical properties of carbon fibers and mechanisms of oxygen functional group according to surface treatment conditions were identified.

For chemical and thermal desizing [1], chemical, thermal, and mechanical properties were analyzed according to the treatment conditions, and for surface treatment [2], FE-SEM, UTM, FT-IR, XPS, BET, and IFSS were performed to evaluate the properties according to the treatment conditions. In addition, during resizing, change of weight, FE-SEM, TGA, AFM, FT-IR, XPS, and IFSS were used to analyze changes in properties according to the concentration and processing time of the resizing agent. In the case of desizing, the sizing agent was completely removed by treatment with acetone for 0.5 h at 60 ^{o}C. At this time, the oxygen of the sizing agent was removed from the surface of the carbon fiber, and the oxygen functional group decreased. During surface treatment after desizing, treatment with nitric acid at 100 ^{o}C for 1 hour was the optimal condition in which the oxygen functional group and the interfacial bonding strength with PA6 significantly increased without changing the tensile properties compared to the carbon fiber before surface treatment (Fig.2). In the case of resizing, at a concentration of 1 wt.% of the PA6-based sizing agent and a treatment time of 10 seconds, 1 % of the sizing agent was coated on the surface of the carbon fiber, and the oxygen functional group and interfacial bonding strength were also at their maximum.

The results of this study showed that surface treatment of carbon fibers exhibited mechanical/thermal/chemical properties equivalent to or better than commercial carbon fibers. Afterwards, we plan to compare and evaluate mechanical properties by manufacturing carbon composite materials by impregnating surface treated recycled carbon fiber under optimal conditions with thermoplastic resin.

Keyword: Recycled carbon fiber, Desizing, Surface Treatment, Resizing, Interfacial bonding strength, Oxygen functional group

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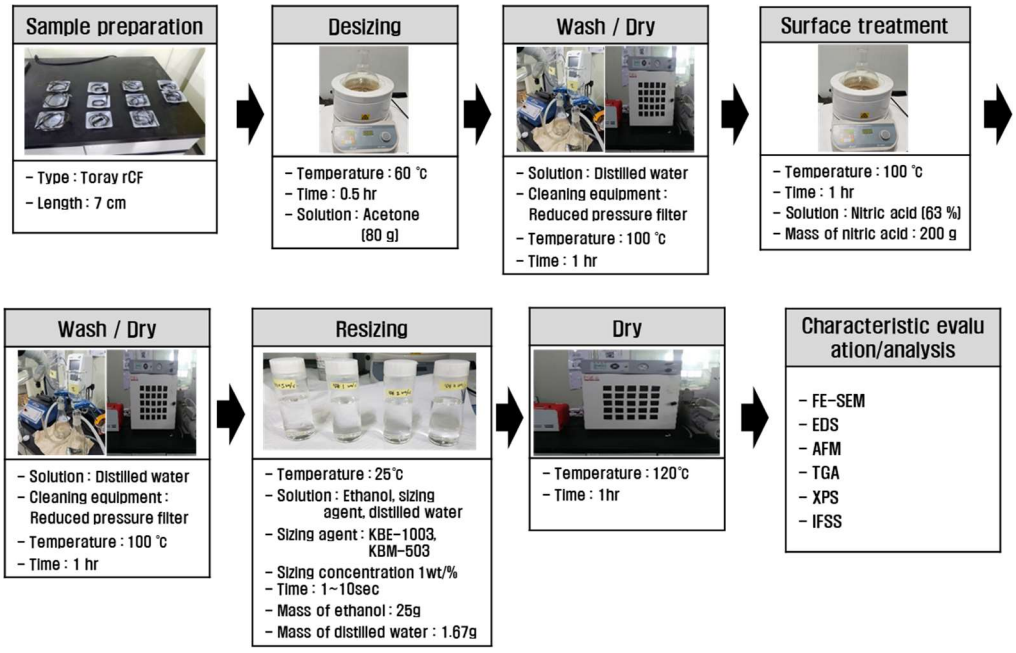

Figure 1. Experimental procedures for desizing, surface treatment and resizing treatment.

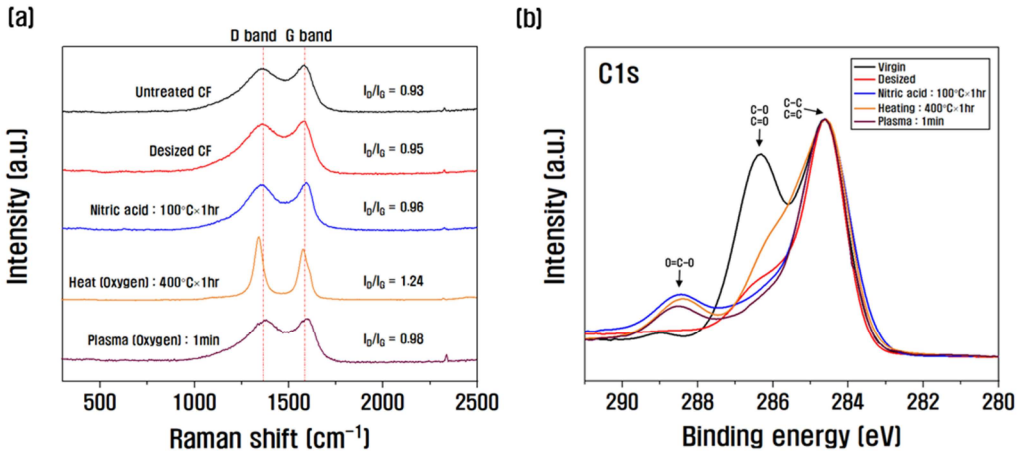

Figure 2. Raman spectra, and C1s X-ray photoelectron spectra of carbon fiber subjected to desizing and surface treatment under different conditions: (a) Raman spectra; (b) X-ray photoelectron spectra.

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Ohmic contact deposition on InGaAs/InP for Si-CMOS compatible HBT fabrication

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To prevent future saturation of the 5G network, the next generation with higher bandwidth must be prepared. A frequency spectrum extending up to 300 GHz has been identified as usable for 6G. Power amplification operating at these high frequencies will be necessary in future systems or Front-End-Modules. Technologies based on InP would enable power amplifiers (PAs) to reach the 300 GHz range [1]. Transistors with $f_{max} \geq 1\,\mathrm{THz}$ then become mandatory in the design of such PAs. HBT-InP transistors are excellent candidates in this regard. The THz threshold has been surpassed in the state of the art with good voltage handling [2][3]. However, these technologies are implemented on expensive and brittle III-V substrates, available in the form of small-sized wafers, thereby limiting integration possibilities with commonly used interconnection solutions for lower-frequency systems. Development of an HBT-InP process integrated on a large-scale silicon substrate must then be considered.

Integrating InGaAs/InP stacks with dielectrics and achieving excellent ohmic contacts using Si-CMOS compatible metallizations are then challenges to overcome. For instance, specific contact resistivities as low as $\rho_c = 2{,}1 \cdot 10^{-5}\ \Omega.\mathrm{cm}^2$ and $\rho_c = 3{,}7 \cdot 10^{-6}\ \Omega.\mathrm{cm}^2$ on p^+-InGaAs have been obtained in other work [4], using respectively Ti and Ni as contact metals. Energy band diagrams of Ti/p^+-InGaAs and Ni/p^+-InGaAs contacts show that Ni is indeed expected to provide a less resistive contact (Fig. 1). However, lower values ($\rho_c \leq 10^{-8}\ \Omega.\mathrm{cm}^2$) are necessary for the emitter, base and collector contacts of the HBT-InP to obtain frequency performance beyond THz. Additional studies aiming to characterize and improve Si-CMOS compatible ohmic contacts have therefore been considered.

TLM structures with 100x100µm contacts are fabricated on InGaAs/InP coupons (insulating substrate) via lithography and lift-off integration, using a two-level mask. Thicknesses ranging from 5nm to 20nm of Ti, Mo, W and Ni have been tested to contact n^+- and p^+-$In_{0.53}Ga_{0.47}As$. The doping concentrations are $N_d = 5 \cdot 10^{19}\ \mathrm{cm}^{-3}$ and $N_a = 8 \cdot 10^{19}\ \mathrm{cm}^{-3}$. A 8nm TiN capping is deposited on Ti and W, but not on Mo and Ni. Formation of the contact plots is then finalized by depositing 30nm of Ti and 200nm of Al. Measurements on as-deposited contacts and after 300°C/60s and 400°C/60s annealings under N_2 atmosphere have been done. Typical specific contact resistivity value on p^+-InGaAs is $\rho_c = 2{,}93 \cdot 10^{-5}\ \Omega.\mathrm{cm}^2$ and is obtained with as-deposited Mo/Ti/Al (Fig. 2). Typical value on n^+-InGaAs is $\rho_c = 1{,}12 \cdot 10^{-5}\ \Omega.\mathrm{cm}^2$ with as-deposited W/TiN/Ti/Al and Ni/Ti/Al metallizations (Fig. 3).
TLM structures with much lower contact dimensions (from 350nm to 5µm) are formed on InGaAs/InP stacks integrated with dielectrics on a 200mm silicon manufacturing platform. A Ti/TiN/W/Ti/AlSi metallization is deposited to contact the n^+- or p^+-InGaAs layer, with the same doping concentrations specified earlier. Measurements have been done, but interpreting the resistivity results is not straightforward as the calculated transfer lengths turn out greater than the contact dimensions. This implies that the limits of the usual TLM interpretation are reached. A COMSOL simulation is therefore being developed to compare the electrical results obtained by TLM extraction with those obtained by simulation. Reproduction of the measurements conditions and of the InGaAs/InP stacks integration into the dielectric/silicon environment is being worked on before starting the simulations (Fig. 4).

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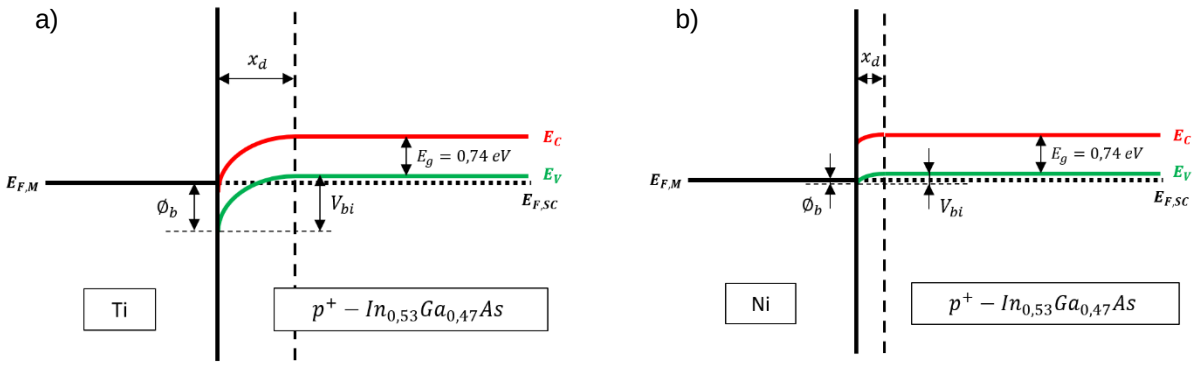

Fig. 1: Energy band diagrams of (a) Ti/p$^+$-InGaAs and (b) Ni/p$^+$-InGaAs contacts (N_a = 8.10^{19} cm^{-3}). Fermi level pinning by surface states is not considered.

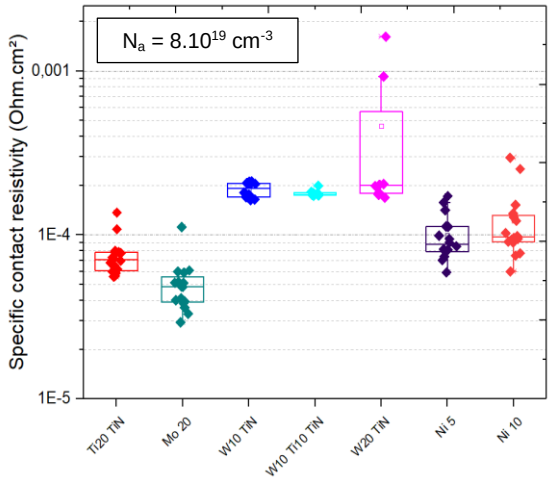

Fig. 2: Measured resistivities of as-deposited Si-CMOS compatible contacts on highly p-doped InGaAs.

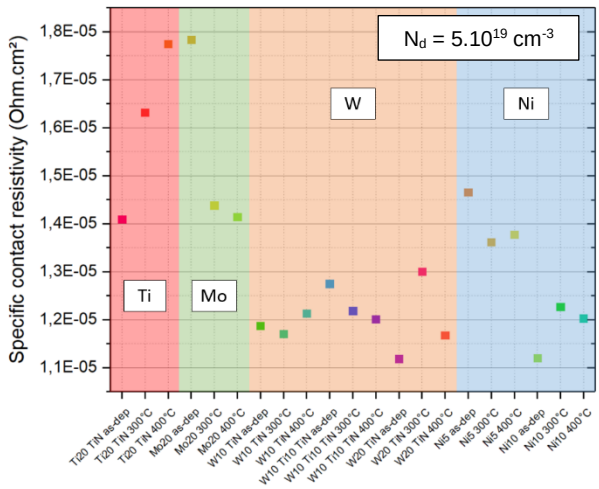

Fig. 3: Measured resistivities of as-deposited and annealed Si-CMOS compatible contacts on highly n-doped InGaAs.

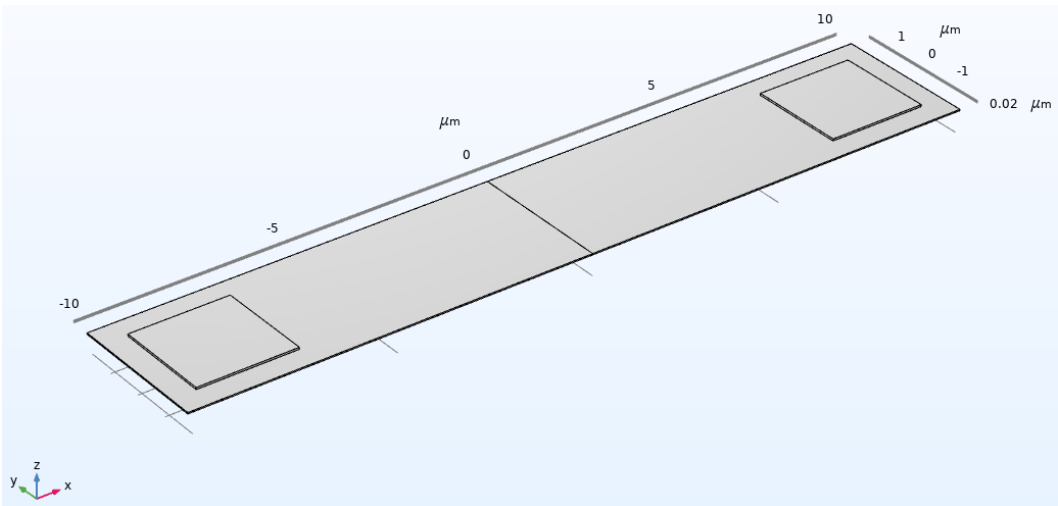

Fig. 4: Reproduction of the TLM structure geometry in COMSOL.

Dopant activation by UV laser annealing to form non-alloy ohmic contact on n+ GaN

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The fabrication process for making ohmic contact on GaN always remains a challenge. For N-type GaN, the traditional alloy type ohmic contact requires high temperature annealing which may introduce material surface roughening [1]. While to form the non-alloy type ohmic contact needs epitaxial regrowth of the heavily N-doped layer, which is time-consuming and costly [2]. Therefore, it is of great interest to explore new process to realize low resistivity ohmic contact for GaN devices [3]. In this paper, we report the formation of non-alloy N-type ohmic contact on GaN achieved by ion implantation and laser annealing. The successful activation of the ion implanted Si dopants (concentration in the order of $10^{20}/cm^3$) in GaN enables the low contact resistivity in the order of 10^{-6} ohm-cm^2.

The experiment is carried out on 6-inch GaN wafers grown by MOCVD. 4 µm of GaN has been grown on Si (111) substrate with an AlN buffer layer. Then a capping layer of 5 nm AlN/40 nm SiN is deposited on GaN for surface protection. Si dopants are implanted at 500°C, with a dose of 4 x10^{15} /cm^2 and a targeted project range of 50 nm. The whole wafer is then annealed by the UV nanosecond laser tool (SCREEN-LASSE LT-3100, 308 nm wavelength, pulse 100-200 ns) at room temperature under air ambient. To characterize the annealed samples, the 4-point probe measurement of sheet resistance (R_s) is firstly performed after removing the AlN/SiN capping. The non-annealed as-implanted reference sample gives unmeasurable R_s. While the R_s of laser annealed samples demonstrate significant reduction. Fig 1 plots the R_s of 7 samples on the same wafer processed using 7 different annealing conditions. We can see that by increasing total laser annealing duration, the R_s of the targeted material decreases to as low as several hundreds of ohm/sq. Both reference sample and the annealed samples were also characterized by AFM after SiN capping removal. Fig 2 presents the surface morphology of the reference sample and the sample A marked in Fig 1 (Rs = 547 ohm/sq) for comparison. The sample A has received the maximum thermal budget in this study, and there is no drastic material surface change caused by laser annealing process. The sample B marked in Fig 1 (Rs = 665 ohm/sq) has been further processed to fabricate an ohmic contact transmission line (TLM) test structure with metal pad spacings of 5 µm, 10 µm, 20 µm and 36 µm. Cl_2-based inductively coupled plasma (ICP) mesa etching of GaN was performed to isolate the TLM test structure, Ti/Al/Ni/Au (20 nm/120 nm/25 nm/100 nm) was deposited by electron beam evaporation to form the metallic ohmic contact. In Fig 3, the linear characteristic of resistance values with respective to different metal pad spacings indicates that a good ohmic contact has been formed between metal and semiconductor. Contact resistance is then extracted by Least Square Method. As shown in Fig 4, the contact resistance is 4.16 ohm-mm with a transfer length of 1.16 µm. The contact resistivity is finally evaluated as 7.48 x10^{-6} ohm-cm^2.

Though more analysis is needed to deepen the understanding, we may conclude that by employing the UV laser annealing of implanted Si dopants to achieve highly N-type doped GaN is a viable technique to form low-resistivity metallic ohmic contact.

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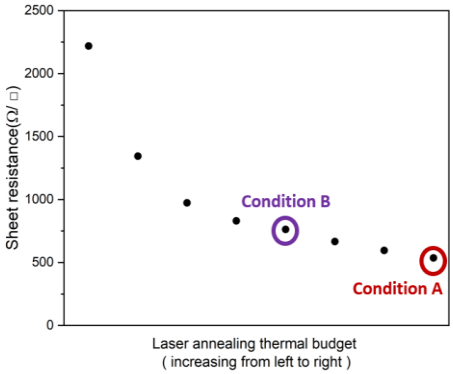

Fig 1. The sheet resistance of laser annealed samples decreases monotonically with the increasing thermal budget applied by laser.

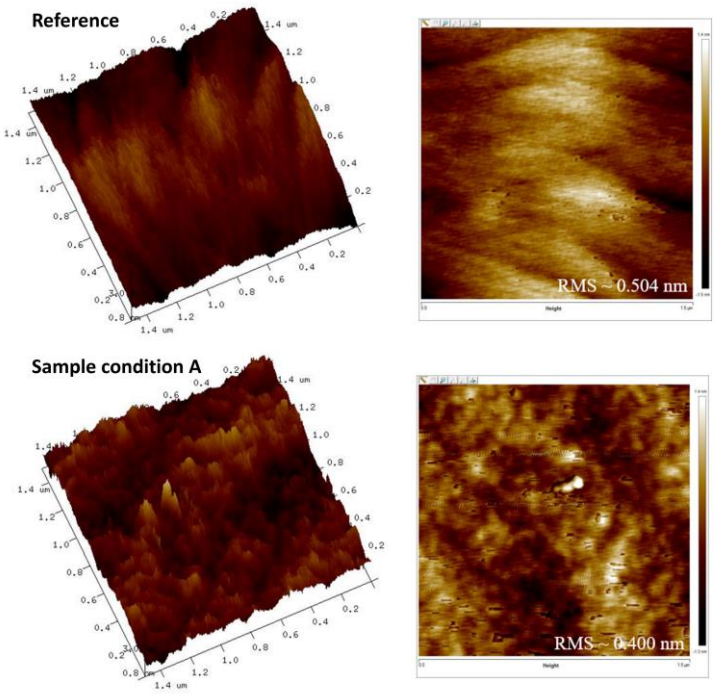

Fig 2. AFM characterization of the reference sample (as-grown without laser annealing) and the sample A marked in Fig 1. It is confirmed that the proposed laser annealing process will not damage the material.

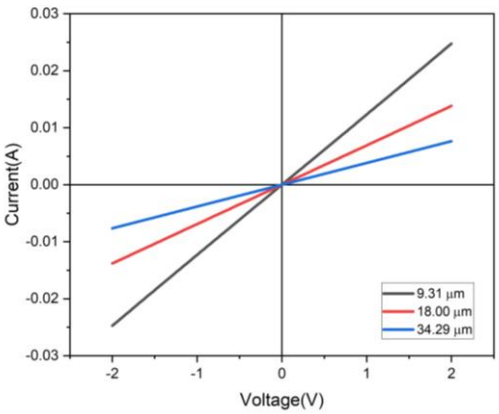

Fig 3. I-V characteristics of TLM structures as metal stack deposited.

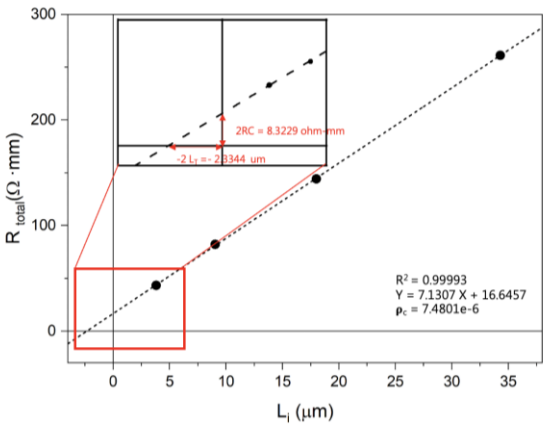

Fig 4. Contact resistance from TLM (Sample condition B). Resistance versus distance between contact pads, L_i, is plotted.

Characterization of highly selective dry etching of pGaN over AlGaN

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GaN-based high electron mobility transistors (HEMTs) are a class of devices based on the electron properties of stacks of doped and undoped gallium nitride and AlGaN alloys. Within such structures, a 2D electron gas (2DEG) is formed, resulting in devices with very low resistivity and improved performances.
The basic structure of those devices consists of a GaN-AlGaN junction with with p-doped GaN gates on top. Dry etching of pGaN selectively landing on AlGaN is a common patterning process to define the gate of the transistor in a normally-off device [1]. To preserve the electronic properties of 2DEG, dry etching must be able to safely remove residues without damaging the underlying layer.
The conventional fabrication technique is based on chemically selective etching step [2], landing on AlGaN after most of the pGaN is removed by a faster and non-selective process. The non-selective step is typically obtained with chlorine-based plasma, whereas the selective process is reached by employing Cl_2 and N_2, where the selectivity is provided by a small amount of added O_2. The process is performed in an ICP reactor from Lam, equipped with two RF generators to sustain the plasma and to set up the ion bombardment independently.

In this work, we present a full characterization of the above-mentioned selective steps, mainly focusing on the study of the sensitivity to the process parameters. Process outcome is characterized in terms of residual AlGaN thickness measured by ellipsometry, in-line nondestructive plan view SEM inspection, and cross section by TEM.

Sensitivity to process parameters

Among all the tunable parameters of the selective step, the most critical are Bias Voltage and oxygen flow. As the final electrical properties of the device depend on the integrity of the AlGaN layer, a highly selective step (high oxygen flow) with low plasma damage (low bias voltage) is required. A drawback of reducing BV and increasing O2 flow is that, besides improving selectivity, the etch rate of the step dramatically drops, resulting in residues or even etch stop, even with small variations.
As for the impact of BV, we found a very narrow window around a possible center point. On the one hand, reducing the voltage rapidly leads to residues formation and etch stop; on the other, increasing it produces excessive AlGaN damage and recess, degrading the final device properties.
As for oxygen, despite increasing its flow provides a more selective step, the corresponding reduction of the etch rate is so strong that heavy residues appear. On the other side, a reduction of the flow may be critical due to selectivity loss at lower oxygen concentration. A thorough explanation of the characterization trials will be provided in the final work.

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Chloroform-Assisted Selective Metal Deposition on Nanopatterned Polymer

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We proposed a new chloroform-assisted selective metal deposition method on polymer nanopatterns for plasmonic device which is fabricated by nanoimprint. To ensure high nanoplasmonic performance, adhesion of the dielectric-metal interface plays a crucial role. However, the poor adhesion property between the UV-curable resin and metal makes selective metal deposition too difficult during imprinting [1].

To solve this problem, chloroform was introduced. Chloroform acts as a mediator, forming van der Waals bond between UV-curable resin and metal, facilitating the transfer of metal thin film to the nanopatterned polymer during UV-imprinting. The pre-UV exposure step provides additional activation energy to reinforce the chloroform-metal bond, preventing chloroform from quickly vaporizing before subsequent processing after coating the metal thin film with chloroform (Fig. 1).

As a demonstration, 8cm x 8cm scale nanostructure is fabricated that features 50nm Ag thin film is deposited on polymeric nanopattern to enable fidelity with <5% (Fig. 2). To evaluate the adhesion characteristic of Ag selectively deposited on nanopatterned polymer, we measured optical intensity [2]. As a result, the interface bonded using chloroform showed relatively excellent properties.

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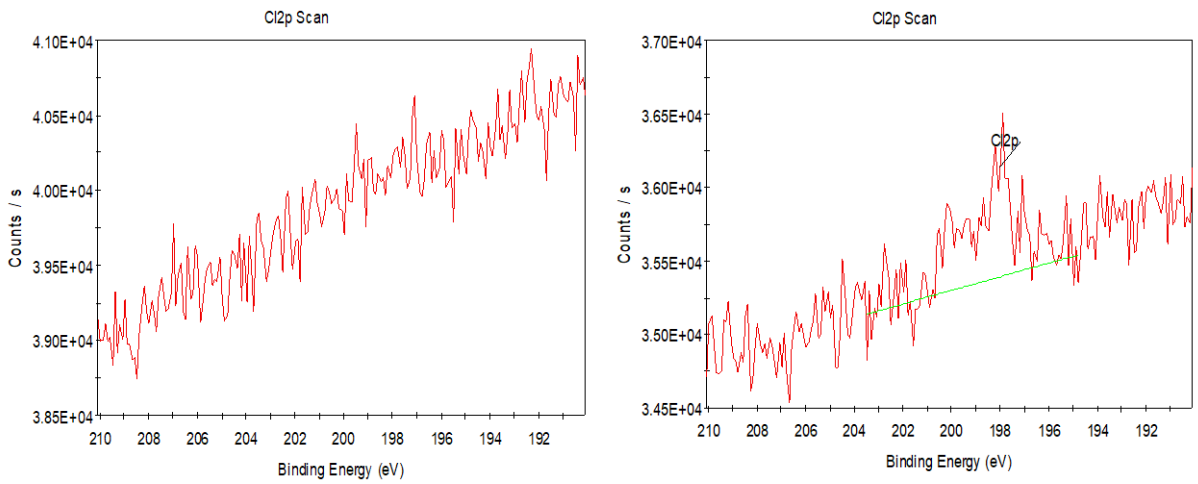

Figure 1. Characterization of pre-UV exposure step

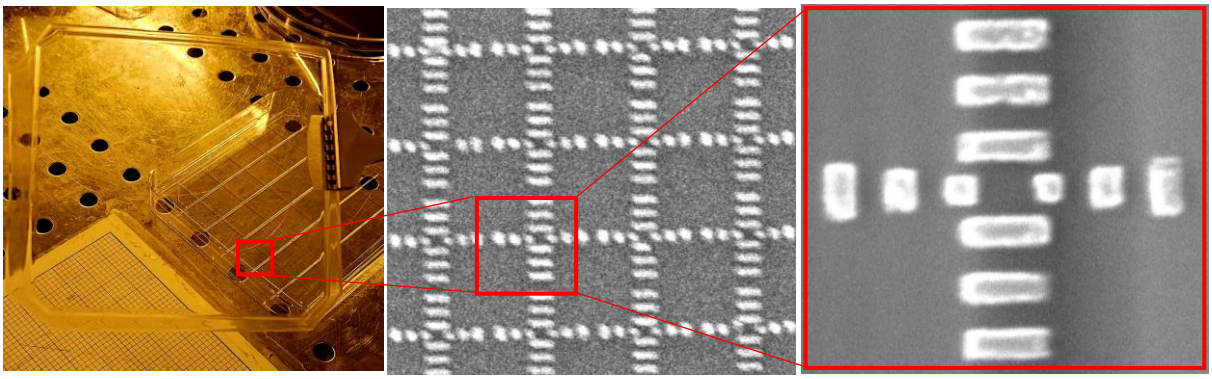

Figure 2. Images of fabricated nanoplasmonic structure

Ohmic contact formation for HEMT device: how to avoid AlN formation in an Al/Ti/Si_3N_4 thin film system

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Ohmic contact formation in HEMT Power GaN device is one of the key aspects for On Resistance (Ron) improvement. The performance of the ohmic contact is influenced by the type of metal stack, the passivation layer in contact with the AlGaN/GaN heterostructure and the thermal treatment used to activate the ohmic contact. In this work we would like to present a study involving these factors, showing some peculiar reactions occurring among the different materials during thermal treatment activation.
Starting from the passivation layer, four different silicon nitride (SiN_x) layers were prepared by means of PECVD technique (Plasma Enhanced Chemical Vapor Deposition) through the modulation of some process parameters during the deposition. Fourier Transform Infrared Spectroscopy (FTIR) measurements were carried out to qualitatively determine the concentration of the Si-H and N-H bonds in the nitride films. These layers were then integrated as AlGaN passivation layers in AlGaN/GaN HEMT. Device process flow continues with the fabrication of the ohmic contacts with an Al metal layer deposited through Physical Vapor Deposition (PVD) technique. The metal stack comprises also a thin Ti barrier as bottom layer and a cap layer of Ti/TiN, while the activation is done with a thermal treatment above 500°C. The post-annealing visual inspection showed high roughness and defectivity in the ohmic contact devices prepared with the Si-rich SiN_x. Physical analysis such as TEM and EDX revealed that the nitride layer in contact with the metal stack was completely converted into AlN (Fig. 1). It has been observed that by going from Si-rich to to N-rich nitrides, the conversion of SiN_x into AlN decreases. This phenomenon can be explained as the result of two reactions:

1. During the thermal treatment activation, the Ti barrier reacts with the Si contained in SiN_x. It's reported that above a certain thermal budget the reaction between Ti and SiN_x leads to the formation of Ti silicides, or Si and TiN at interface [1]. As a result, the Ti barrier disappears, and alloys of Ti-Al-Si are formed in the Al metal.

2. Without a proper metal barrier, the reduction of SiN_x by Al can take place, forming AlN and Si (H_{298K}= -126kcal/mol)[2] [2].

   $4Si_3N_4 + Al \rightarrow 4AlN + 3\,Si$

The occurrence of this sequence of reactions is unwanted not only for morphological reasons, but also for the electrical performance of the device as described in the paper.
Indeed, nitrogen rich layers enhance the formation of Ga-N bonds, reducing Si-Ga and Si dangling bonds, thus alleviating leakage currents [3].
However, the nitride stoichiometry is not the only factor involved in the formation of AlN, also the metal layers and the following thermal budget have a significant role. We studied a solution to have an AlN free ohmic contact through the combination of a N-rich SiN_x layer and a proper modulation of the metal stack. The goal is to preserve the Ti layer, so that it is not entirely consumed by the reaction with Si; the Ti acts as a separation between Al and SiN_x, avoiding the starting of reaction 2.

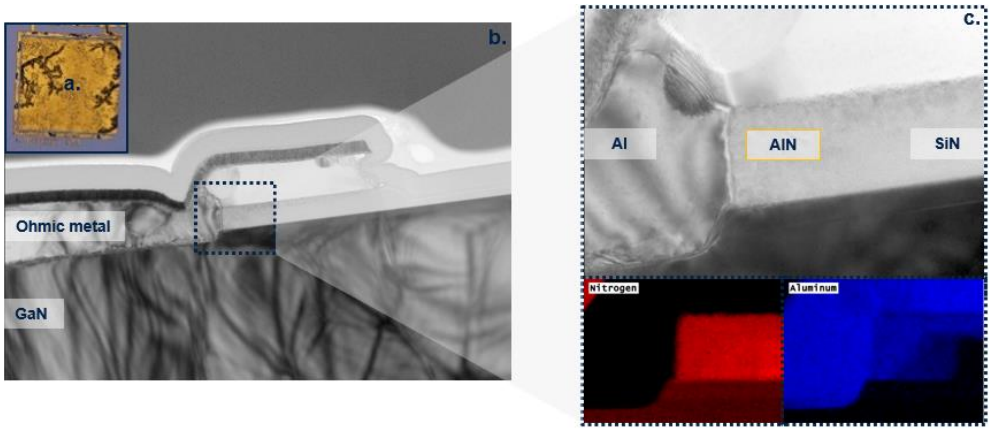

Figure 1 - Optical microscope top view of the ohmic contact after the thermal treatment showing the metal roughness (a). TEM cross section of the ohmic contact (b). Zoomed TEM image of the contact side and EDX analysis showing AlN formation at Al/Ti/ SiN_x interface (c).

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Characterization and Metrology Development of a Copper Plating Bath for High Performance Glass Substrate Interconnect

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Glass is considered as a promising base material used in semiconductor manufacturing. Compared to traditional organic substrates, glass substrates offer excellent physical, mechanical, and optical properties, that enable more transistors connected in one package, higher signal stability at high frequency ranges with lower electrical loss, and better scaling for larger chiplet complexes [1]. These advantages lead to their wide use in various processes of semiconductor manufacturing, such as 3D integration, also known as through glass via (TGV). Since silicon is a semiconductor material, the carriers around through silicon vias (TSV) can move freely under the action of electric field or magnetic field, which will interfere with adjacent circuits or signals and affect chip performance. The glass material does not have free moving charges, and there is no need to deposit an insulating layer. It has excellent dielectric properties. Meanwhile, the thermal expansion coefficient of glass can be adjusted, reducing the thermal mismatch with different materials. Due to the easy availability of large-sized glass panels, the glass cost is about 1/8 of that of silicon substrates. With strong mechanical stability, even when the thickness is less than 100µm, the warpage is still small [2].

Void-free interconnect metallization has been identified as one of the most fundamental processes in TGV due to the concerns of RC delay and reliability [3]. Direct copper plating presents an excellent technique for TGV metallization, because of faster processing, easier implementation, and cost advantages, compared to other wet and dry processes [4]. Due to a high aspect ratio structure, it is common to use complex plating additives to achieve bottom-up filling in direct copper plating [5]. However, the mixed and synergistic effects of organic additives in complex chemistries pose a great challenge to develop robust methods for bath monitoring. Comparing to traditional TSV plating bath, TGV has higher copper concentrations approaching solubility limit, causing bath to operate at elevated temperatures. To obtain accurate results and enable reliable performance of analyzer, precipitation of copper sulfate should be prevented during analysis of plating bath. Plating on glass also require special equipment, which is different to traditional plating tools for TSV metallization. Electrochemical and hydrodynamic conditions of these devices cause specific consumption of bath components. The difference in consumption rates dictates more often analysis for some bath components, e.g., brightener.

Analytical methods that are both accurate and reproducible are extremely important to monitor and maintain a healthy plating baths, as the constituents in a plating bath must be controlled in specific concentration ranges to attain desired deposit properties. To develop such analytical techniques, the interactions among organic additives of a commercial copper acid chemistry were investigated in this study. The additives include a strong polarizer (carrier), a depolarizer (brightener), and a leveling agent (leveler) which is not typical for traditional TSV baths. The commercial chemistry is applicable for through hole with both X shape and mechanical drill through hole as well as large size blind via as shown in Figure 1 [6]. The responses of organic constituents under different electrochemical and hydrodynamic conditions were examined, and the results suggest the carrier, brightener and leveler exhibit very prominent polarizing, moderate depolarizing, and weak suppressing effects, respectively in Figure 2A. A comparison between Figure 2B and 2C indicates that these components are more sensitive to mass transfer rate (Figure 2C) than kinetics (Figure 2B). Optimized electrochemical analytical techniques was developed for the commercial chemistry and the analyses were performed with simple and automated fluidics that include a single electrochemical cell and accurate temperature control. The analysis performance was evaluated in terms of accuracy against its expected concentration and repeatability, which is summarized in Table 1.

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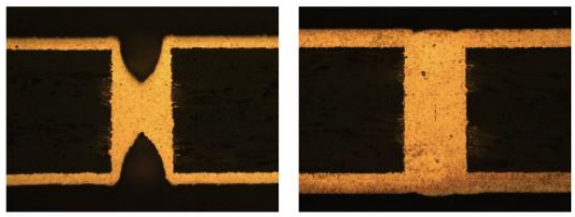

Figure 1 Metallographic images of through hole deposit by the commercial acid copper chemistry [5]

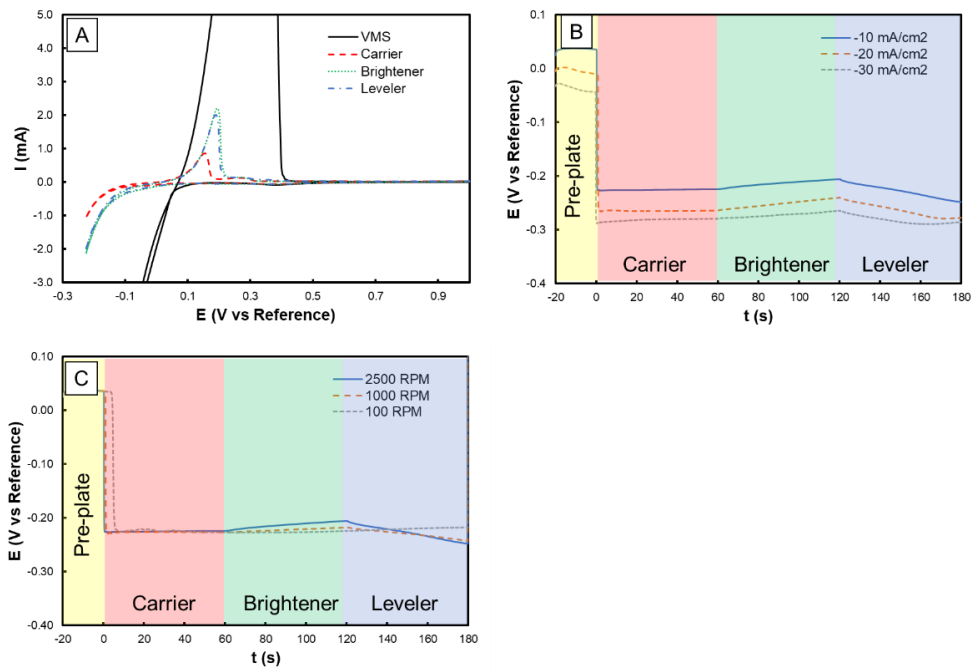

Figure 2 (A) Voltammogram in the commercial chemistry in presence of carrier, brightener, and leveler, (B) effect of organic additives on chronopotentiogram at varying current densities (2500 RPM), and (C) effect of organic additives on chronopotentiogram at varying rotation rates (-10 mA cm^{-2}).

Table 1 Online Performance of analytical techniques of the commercial chemistry for glass substrate plating

Component	Carrier	Brightener	Leveler
Accuracy	<3%	<1%	<0.5%
Repeatability	<1%	<2%	<1%
Analysis Time (min)	<10	<15	<15

TiAl3 for W CVD chamber temperature measurement

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Since the critical dimension of integrated circuits has shrinked, tungsten CVD deposition, thanks to its better step coverage with respect to Aluminium PVD one, has become the metallization technology of choice for filling of contacts and vias. [1]
This technique is based on the chemical reduction of tungsten hexafluoride. The deposition process consists of two main steps: nucleation, with silane and hydrogen as reducing agents, and bulk deposition, with H_2 as the only participant, basing on formulas (Eq.1) [2].

Among the various process parameters that are involved in the reaction, pressure, gas flows and temperature play a key role in the process control.
While for pressure and gas flow there are several methods to measure and control in real time their values, such as manometers and flowmeters, regarding temperature the only way we have to control it is based on a thermocouple reading below the heater which has main drawback the fact that it can not measure the real temperature on the wafer.

The aim of this work is to provide a quick, simple and consistent method to control temperature at wafer level.

In the kinetic limited regime, the deposition rate (R) is independent from WF6 flow, but it is a primarily a function of the wafer surface temperature and hydrogen partial pressure as expressed in the Arrhenius equation (Eq.2) [3].

Being deposition rate dependent on temperature, with the shrink of critical dimensions and the increase of aspect ratio severities, it has become critical to fine control the temperature in order to guarantee an optimal structure filling without the formation of any voids. (Fig.1)

$TiAl_3$ temperature control method is based on kinetic of $TiAl_3$ formation, starting from Ti and Al reagents (Eq.3).

A wafer with a layer of Ti and a layer of AlCu(0.5%) is introduced in a hot chamber for a fixed time.
At the chamber process temperatures (above 400°C) TiAl3 formation begins, causing a resistance sheet increase [4].
By measuring the difference between resistance sheet before and after heating the wafer, we can indirectly obtain the temperature of the process chamber (Eq.4).

This work focuses on building a new calibration curve to better fit and adapt the method to MCVD Centura WxZ chambers and statistically verifying new method consistency and accuracy.

The new calibration curve was obtained by using a thermocouple (TC) wafer as reference.
Thermocouple wafer is an alternative method to measure process chamber temperature, it is very precise and reliable, however it requires long chamber downtime thus impacting manufacturability.
Heater temperature was measured by TC at four different setpoints and the new calibration curve coefficients were extrapolated (Fig.2).
Once the curve was built, reproducibility and repeatability were confirmed by means of GaugeR&R method on five different process chambers.
Linear regression curve was used to verify the consistency between computed temperatures and deposition rate of chambers (Fig.3).
Finally, method resolution was confirmed by forcing a 5°C and 10°C shift setpoint and by demonstrating the results were statistically distinguishable through Anova methodology (Fig.4).

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Equations

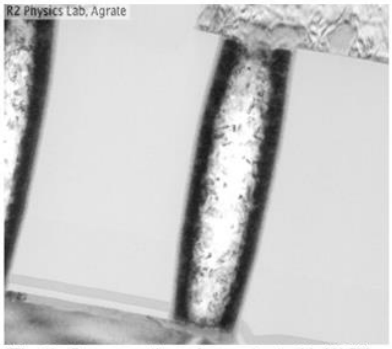
1. $3\,H_2 + WF_6 \rightarrow W + 6\,HF$
   $3\,SiH_4 + 4\,WF_6 \rightarrow 4\,W + 3\,SiF_4 + 12\,HF$

2. $$R = K\sqrt{P_{H2}}\,e^{\frac{-Ea}{RT}}$$

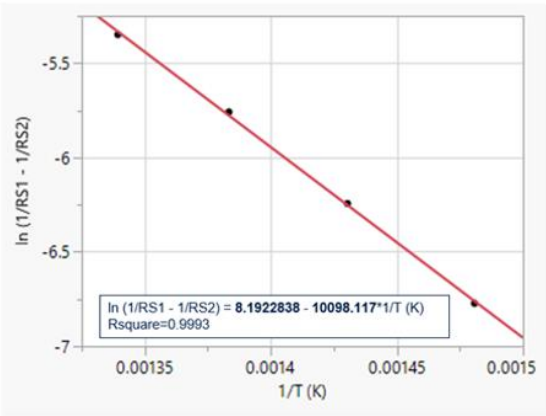
3. $Ti + 3\,Al \rightarrow TiAl_3$

4. $$\frac{1}{T} = \frac{\ln\left(\frac{1}{RS_{pre}} - \frac{1}{RS_{post}}\right) - \beta}{\alpha}$$

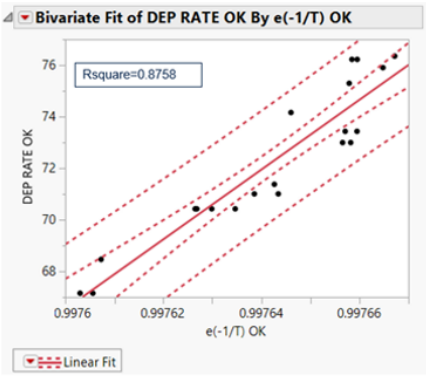
Figures



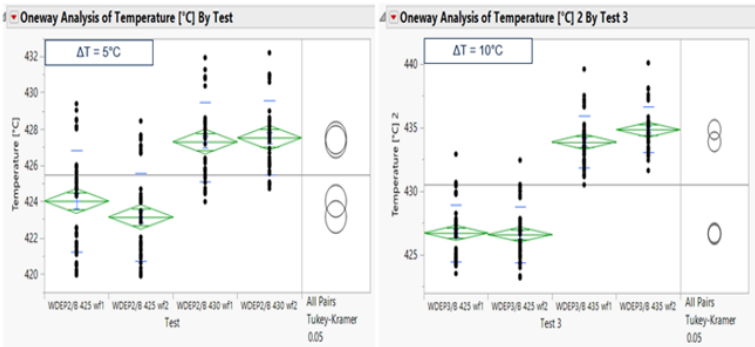
(Fig.1): Cross section of a contact with W filling problem.



(Fig.2): calibration curve with extrapolation of new calibration coefficients



(Fig.3): linear regression of deposition rate as a function of temperature



(Fig.4): Anova anlysis for 5°C and 10°C differences

Strategic Superposition: Sb2Te3/TiTe2 Superlattices Possess a Low Thermal Conductivity Contrast, Ideal for PCM

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Introduction

Reducing the energy consumption of phase change memory (PCM) is one of the biggest hurdles towards its implementation. The switching mechanism in PCM consists of applying enough heat to the material to change it from crystalline to amorphous or vice versa. Diffusion of this heat into the surroundings of the cell is therefore detrimental. The thermal conductivity of the phase change material and its surroundings plays a crucial role in reducing the energy needed for a PCM to function. A good PCM material should have low thermal conductivity in both its crystalline and amorphous phase. Typical materials such as GST on the other hand, display a significant contrast in their thermal conductivity [2]. As a possible improvement we study $Sb_2Te_3/TiTe_2$ superlattices, a material system first proposed by Shen et al. in reference [1] showing a significant reduction in its reset power consumption. After deposition and structural characterization of these superlattices, the thermal transport properties are examined using time-domain thermoreflectance (TDTR).

Methods

All samples are created through magnetron co-sputtering from elementary pure targets in a variation of the modulated reactants method [3]. This method has been shown to create high-quality and planarly texturized layers with the *00L* family of planes parallel to the substrate upon crystallization. This is verified through *in situ* and *ex situ* XRD and rocking curve analysis. Time-domain thermoreflectance (TDTR) measurements are performed in a two-tint setup. This a laser pump-probe technique with which the cross-plane thermal conductivity of thin films can be accurately measured. These measurements are performed at room temperature for different thicknesses and at increased temperatures under an inert atmosphere to study the evolution of the thermal conductivity upon crystallization.

Structural Characterization

XRD patterns for films of the individual materials as well as their superlattice can be seen in figure 1. The intensity and presence of the *00L* peaks are indicative of a strong crystalline texture of the films. The evolution of an as-deposited superlattice upon anneal is visible in figure 2. Crystallization and melting of Sb_2Te_3 are visible. The intense satellite peaks are indicative of the layered structure [4].

Thermal Conductivity Results

TDTR results of single-layer samples of the individual materials are shown in figure 3. Both materials show a relatively low thermal conductivity in their as-deposited state, while (further) crystallization upon anneal increases it. The *in situ* data for a single 80nm Sb_2Te_3 layer can be seen in figure 4 where it is presented next to data for 16-period thick superlattices. A set of three types of superlattice is studied: 5nm of Sb_2Te_3 is combined with either 3nm, 6nm or 9nm $TiTe_2$. At room temperature we see that the relative composition has little effect on the as-deposited samples. This can be explained by the high thermal resistance of the amorphous Sb_2Te_3 sub-layers that dominate the stack. During anneal the thermal conductivity of all superlattices increases. Although upon cooling down, the value for the 5-3 superlattice drops down to the same value as before the anneal, reducing all contrast in thermal conductivity between the crystalline and amorphous phase.

Conclusions

The superlattice consisting of 5nm Sb_2Te_3 and 3nm $TiTe_2$ shows a minimal contrast in thermal conductivity between its two phases at room temperature, making it better suited than a single layer of Sb_2Te_3 for use as a phase change material. All superlattices demonstrate a lower thermal conductivity than the bulk as well as a decreased contrast. This might indicate that the superlattice's added interfaces not only introduce a thermal resistance, but also influence the phononic landscape, leading to the low thermal conductivity contrast that is observed.

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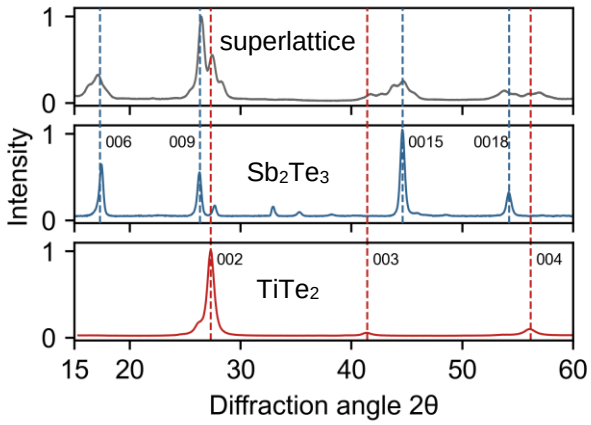

Fig. 1: The XRD pattern of an annealed superlattice shows peaks of both bulk Sb_2Te_3 and $TiTe_2$. The presence of satellite peaks is indicative of the superlattice structure.

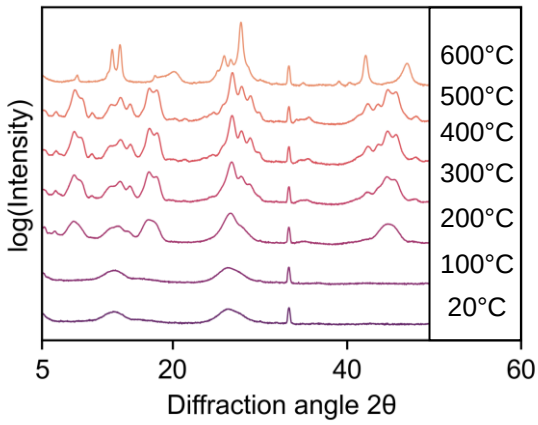

Fig. 2: *Ex situ* scans of a superlattice annealed at different temperatures show the crystallization and subsequent melting of Sb_2Te_3 .

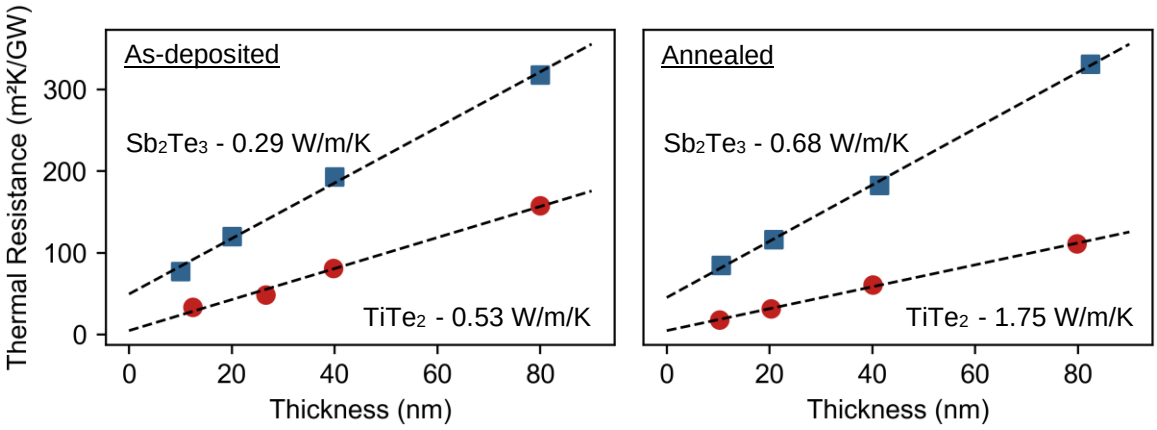

Fig. 3: The intrinsic thermal conductivity of the single layer materials is calculated by combining results for several thicknesses and performing a linear fit. These results show the thermal conductivity contrast between as-deposited samples and after a 300°C ramp anneal.

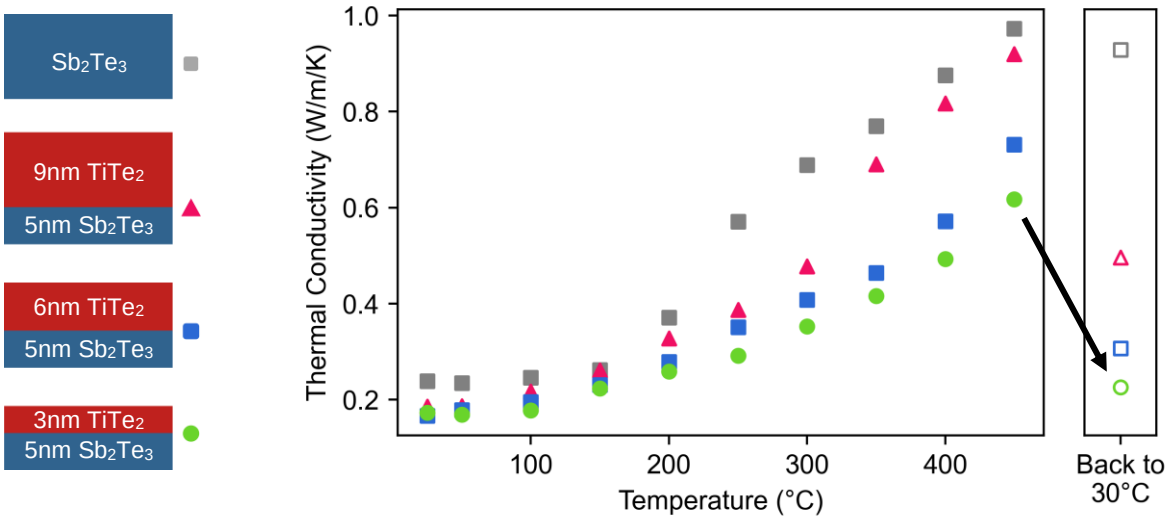

Fig. 4: Three types of superlattices are compared to bulk Sb_2Te_3 during *in situ* TDTR measurements. Thermal conductivity increases for all samples when heating up. After cooling down the 5-3 superlattice still shows a very low thermal conductivity, despite its crystallinity.

Hydrogen role in GaN based semiconductors: ToF SIMS profiles and resistance study.

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In recent years, the demand for electric power has been on the rise, leading to a shift in focus towards wide band semiconductors (WBG), such as gallium nitride (GaN) and its related alloys. One of the most interesting aspects of GaN materials is the ability to grow AlGaN/GaN heterostructures, which form a two-dimensional electron gas (2DEG) and allow for the design of AlGaN/GaN high electron mobility transistors (HEMT) structures. However, a major challenge with this technology is its normally-ON nature, which limits its applications. To improve system reliability, normally OFF HEMTs are highly desirable. One method to achieve this goal is to grow a p-type cap layer (pGaN) using magnesium (Mg) as the most used acceptor [1]. Mg-doped GaN is grown using metalorganic vapor deposition (MOCVD), with metalorganics and organic compounds and hydrides as precursors (ammonia NH_3, Trimethylgallium - TMGa, and biscyclopentadienyl-magnesium - Cp_2Mg), and the growth usually occurs in H_2 ambient. This results in the presence of Mg-H and atomic H, which significantly increase the resistance of Mg-doped GaN due to the deactivation of Mg [2]. To activate Mg impurities, thermal annealing is required, which induces hydrogen dissociation from the Mg-H complex in the Mg-doped GaN layers.

Despite the known mechanism, there have been only a few quantitative experimental investigations on the relationship between the amount of hydrogen dissociated from Mg-doped GaN and the electronic properties of the p-GaN. This study aims to address this gap by correlating the role of hydrogen in the thermal activation process of Mg-doped GaN and the resistivity variation of p-GaN, as a function of temperature up to 800°C. Time-of-flight secondary ion mass spectrometry (ToF-SIMS) was used to evaluate the Mg and H depth profiles, and Hall measurements were adopted to investigate the conductive properties of the annealed samples. Through the optimization of ToF-SIMS acquisition protocols (Fig.1), we were able to improve the detection limit of hydrogen and correlate its concentration values with the GaN electronic properties. Specifically, our study utilized Hall measurements and sheet resistance measurements in a Van Der Pauw configuration (Fig. 2) to investigate the activation rate of dopant impurities and their correlation with hydrogen content. Our findings suggest that the activation rate of dopant impurities is not strictly correlated with the concentration of hydrogen present.

These findings have important implications for the development of normally OFF HEMTs and the wider field of WBG semiconductors.

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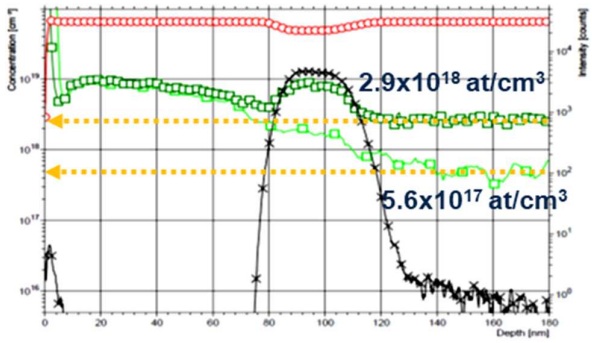

Fig. 1: *H^- concentration profile in the as grown sample obtained by TOF-SIMS analysis operating in interlace mode (light green open symbols) and not interlace-mode (dark green open symbols).*

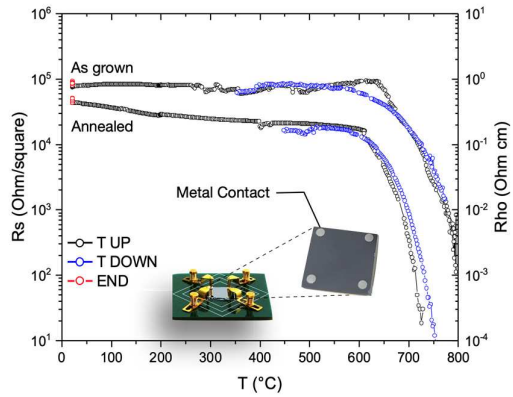

Fig. 2: *Evolution of sheet resistance (Rs) as a function of temperature for the as grown and annealed samples. Measurements were performed in Van der Pauw configuration as shown in the inset.*

Investigating the Evolution of Warpage Hysteresis Loop to Bifurcation Hysteresis Loop in Cu_ECD/Si large Wafers through Finite Element Analysis

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Abstract During the final thinning process, large semiconductor wafers with thick electrochemically deposited copper (Cu_ECD) layers are known to exhibit significant warpage. This warpage can manifest as either an asymmetric warpage or a bifurcation of the wafer. While finite element analysis software can predict this phenomenon, an accurate prediction requires considering the plastic behavior of the metal layer. To address this issue, a study was conducted to extend a finite element analysis multilinear kinematic hardening model of plastic Cu_ECD from a die level to the wafer level. The aim was to predict the warpage hysteresis loop and deduce the phenomenon of bifurcation during the thinning process of a 200 mm standard wafer. The results of this study have important implications for the semiconductor industry, as they offer a means of predicting and mitigating the warpage and bifurcation of large semiconductor wafers during the final thinning process.

Introduction Large semiconductor wafers, such as 200 mm nominal wafers, metalized with thick electrochemically deposited copper (Cu_ECD) layers, often experience significant warpage during the final thinning process. This warpage can degenerate into the bifurcation phenomenon, resulting in an asymmetric warpage of the wafer. While finite element analysis software [1-4] can describe the bifurcation phenomenon, accurately predicting warpage and bifurcation in large Cu_ECD metalized wafers requires consideration of the plastic behavior [5] of the metal layer. The plastic behavior of thick Cu_ECD is evident in the investigation of warpage during thermal cycling, resulting in a warpage hysteresis loop. In this investigation, we extended a finite element analysis multilinear kinematic hardening (MKH) model of plastic Cu_ECD from a die level to the wafer level to predict the warpage hysteresis loop at the wafer level and deduce the phenomenon of bifurcation during the thinning process. We tested the MKH model using experimental data reported in the literature [5] and simulated the warpage hysteresis loop at the die level of 20 µm Cu_ECD thick deposited on a Si (001) die with standard thickness. We then extended the investigation to a 200 mm standard wafer Cu_ECD metalized and compared the resulting curvatures, which were comparable. Finally, we investigated the emergence of bifurcation in thinned silicon wafer substrates.

Results

In fig.1. and 2 we report a schematic of the die and a graph of the thermal cycle utilized to simulate the warpage hysteresis loop (WHL), respectively. In fig.3 we report the comparison of the warpage resulting from the simulations and with the experimental data reported in ref [5]. In fig. 4 we investigated the upscaling of the warpage hysteresis loop by comparing the curvatures gained from the die with those gained from a 200mm wafer having both the same standard thicknesses of 730 µm. It results that the curvatures are comparable and consistent. In Fig. 5 we determined the WHL for the case of thinned wafers. As the thickness of the wafer decreases it results that the curvature increases. Moreover, by probing the resulting directional deformation at +250°C and -50°C, we can observe as the wafer bifurcates with a negative and positive curvature, respectively. In particular, in Fig. 6. we report the distribution of the directional deformation along the z-direction for the case of a wafer having a thickness of 400 µm, when the warpage hysteresis loop reaches the temperature of +250 °C. In fig. 7 we report the distribution of the directional deformation along the z-direction for the case of the same wafer, when the warpage hysteresis loop reaches the temperature of -50 °C.

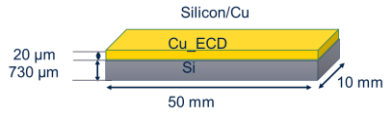

Fig.1. Schematic of a silicon (001) 5cm x 1cm die sample, 730 µm thick metalized with a 20 µm thick copper electrochemically deposited (ECD) layer.

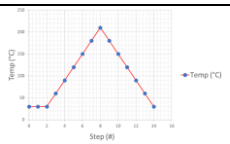

Fig. 2. Thermal Cycle exploited to simulate the plastic behavior of Copper ECD deposited on Silicon.

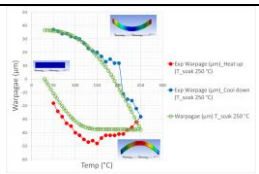

Fig. 3. Graph of the warpage hysteresis loop of a 5 cm x 1cm die Cu_ECD/Si (001) reporting the experimental data where the soak temperature was of 250 °C collected from ref [5] and the comparison with a multilinear kinematic hardening (MKH) model set up with a Ansys mechanical enterprise R2/2023.

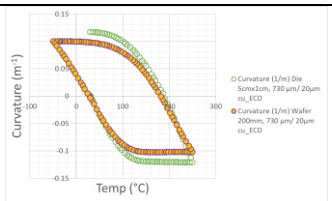

Fig. 4. Comparison of the curvatures gained from the simulated warpage hysteresis loop gained of the die of fig. 3 and that simulated for a 200 mm silicon (001) wafer having a thickness of 730 µm, according to the same MKH model.

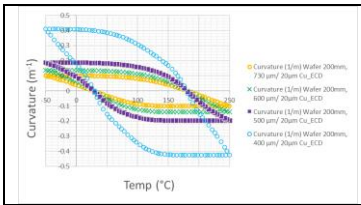

Fig. 5. Increase of the curvature of the warpage hysteresis loop of a 200 mm Si (001) wafer metallized with Cu_ECD 20 µm, modelled according to a MKH model, as the thickness of the wafer decreases from 730 µm to 400 µm.

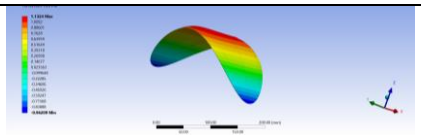

Fig. 6. Bifurcation observed at 250 °C in the warpage hysteresis loop of a 400 µm Si (001) 200 mm wafer metalized with a 20 µm Cu_ECD layer.

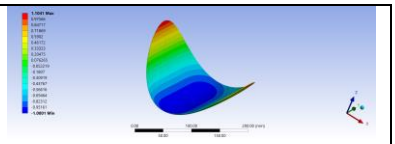

Fig. 7. Bifurcation observed at -50 °C in the warpage hysteresis loop of a 400 µm Si (001) 200 mm wafer metalized with a 20 µm Cu_ECD layer.

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Pre-amorphization implantation (PAI) process assessment for GaN contact technologies

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Ohmic contacts are used in many technologies to connect active parts of electronic devices to back-end circuits. However, achieving low contact resistances on GaN substrates and related materials remains a challenge [1]. Several process steps are required to form a contact, generally including surface preparation, metal deposition, and annealing. In silicon technologies, several levers such as pre-amorphization by implantation (PAI) have been proposed in order to tune the properties of the silicide layer and the associated NiSi/Si interface obtained by silicidation [2]. In such processes, the substrate is amorphized over a few nanometers prior to metal deposition, which affects the subsequent silicide formation mechanisms. Typically, crystalline phase formation temperatures can be modified to induce metallic alloy formation at relatively low temperatures [3]. If such a trend could be obtained on GaN, adapted intermetallic alloys could be developed, with the advantage of mitigating the difficulties of preparing the GaN surface prior to metal deposition.

In this work, the potential of using PAI processes on GaN for power electronic applications is evaluated by implanting non-intentionally doped GaN samples with a single Al shot at 4 keV and 1E16 at.cm^2 (VIISTA HCP implanter from Applied Materials). The sequential deposition of a 30 nm metal (Ni or Ti) layer and a 10 nm TiN capping layer is then performed without air break using an Endura 200mm integrated platform from Applied Materials. Depending on the sample, different thermal budgets are then applied (see Table 1). The resulting samples are characterized by high-angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM) and corresponding energy dispersive spectroscopy (EDS) spectra, out-of-plane (θ-2θ) and in-plane reciprocal space map (IPRSM) X-ray diffraction.

For Ni-based samples, Fig. 1 shows that the use of a pre-implantation step changes the morphology of the contact obtained after annealing at 600 °C. Indeed, while a $Ni_{1-x}Ga_x$ layer (i.e. Ni-rich NiGa) is obtained for both samples, most likely by diffusion of Ga atoms into the Ni layer, only the sample where the substrate was amorphized shows additional areas where Ni atoms seem to have diffused into the GaN substrate. The associated alloy is found to be about 40 nm thick and has a stoichiometry close to NiGa. This difference between samples annealed at 600 °C is confirmed by XRD analysis in Fig. 2. For the reference sample, the obtained IPRSM is composed of a series of epitaxial-like spots consistent with Ni_4Ga, as confirmed by θ-2θ measurements (see Fig. 2.a and Fig. 2.b, respectively). For the sample with PAI, the resulting alloys show a fiber texture, with the presence of Ni_4Ga and NiGa related components (see Fig. 2.c). More importantly, the system evolution is accelerated when the substrate surface is amorphous: for samples annealed at 500 °C, the GaN 002 to Ni_4Ga 111 diffraction line intensity ratio is higher for the reference sample (see Fig. 2.b) than for the implanted one (see Fig. 2.d).

The results described above indicate a promising use of PAI processes for GaN technologies, as will be discussed in detail in this paper. Results for Ti-based samples, which also show differences whether or not a PAI step was used prior to metal deposition, will be presented.

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PAI conditions	Metallization	Annealing condition
None (Ni based samples ref.)	Ni(30nm)/TiN(10nm)	Ar, 3min, 500°C and 600°C
Al: 4keV, 1.10^{16} at/cm²	Ni(30nm)/TiN(10nm)	
None (Ti based samples ref.)	Ti(30nm)/TiN(10nm)	
Al: 4keV, 1.10^{16} at/cm²	Ti(30nm)/TiN(10nm)	

Table 1: Studied samples

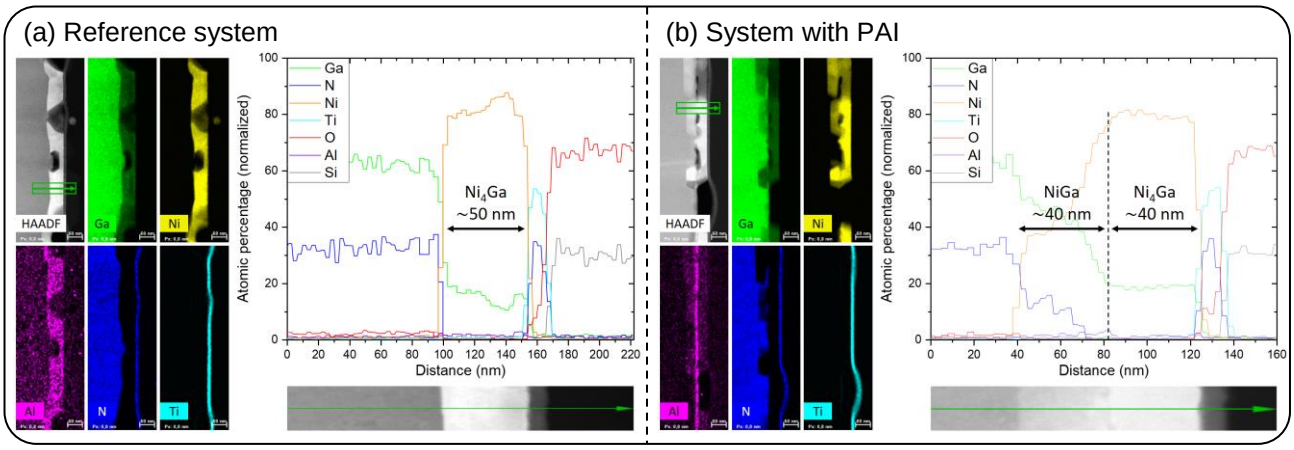

Fig. 1: HAADF-STEM image and corresponding EDS-STEM elemental mappings of the Ni-based system after annealing at 600 °C (a) without and (b) with PAI. For each sample, the composition profile across the stack measured by EDS along the green arrow (see HAADF image) is shown on the right.

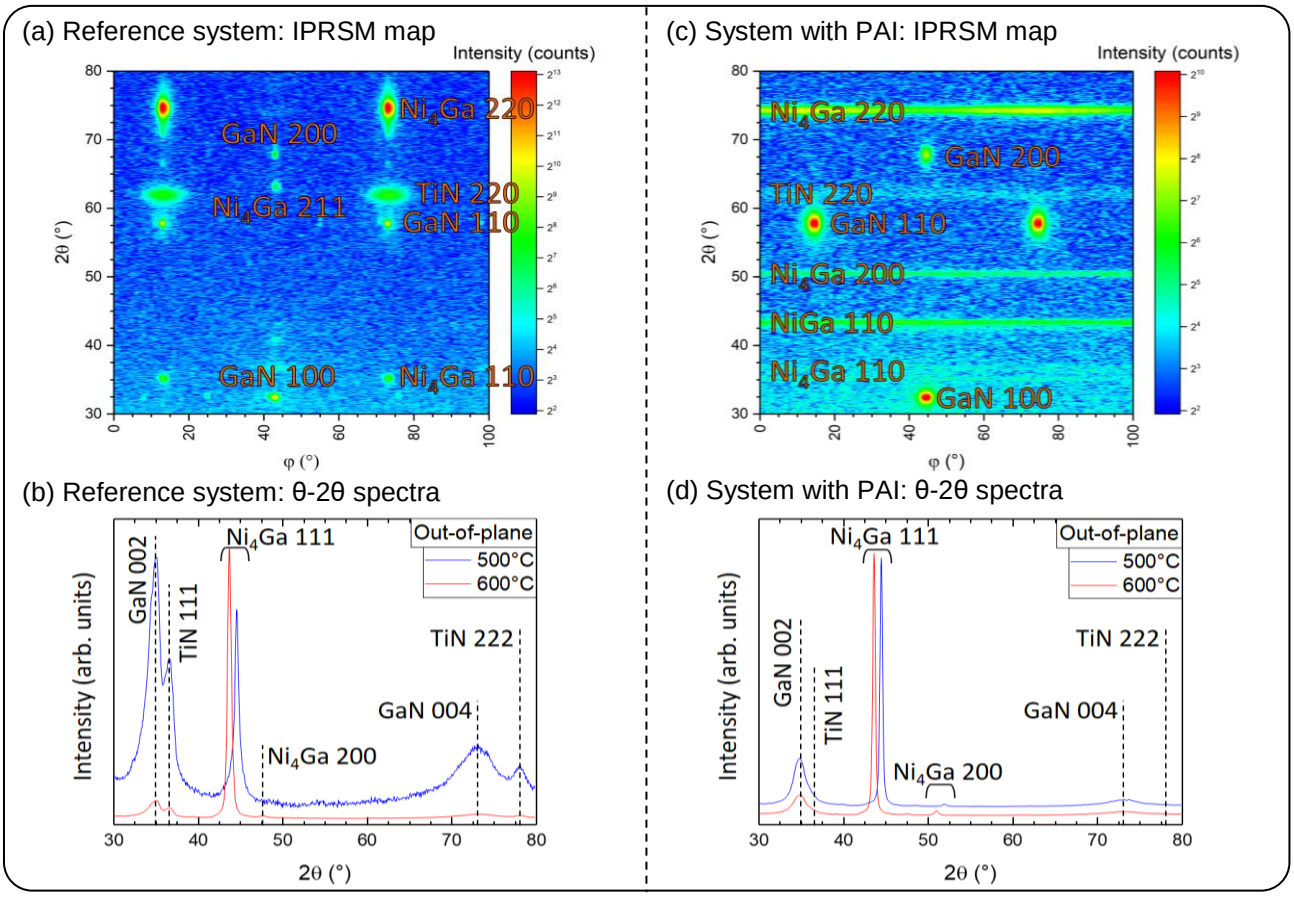

Fig. 2: XRD analysis of the Ni-based system. Figures on the left side (a, b) correspond to the reference sample while those on the right side (c, d) correspond to the system with PAI. (a) and (c) show IPRSM maps after annealing at 600 °C while (b) and (d) show out-of-plane θ-2θ results for two annealing temperatures, 500 °C in blue and 600 °C in red.

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